Sil9573 and Sil9575 Port Processor

Data Sheet

SiI-DS-1089-F

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1. General Description

The Lattice Semiconductor SiI9573 and SiI9575 Port Processor is the latest generation HDMI® port processor targeted at audio video receivers (AVR), Home Theater in a Box (HTiB), and Digital TVs (DTVs). The port processor has many innovative features such as InstaPort®, InstaPrevue, Mobile High-Definition Link (MHL®), ViaPort Matrix Switch (the SiI9575 device only), and Audio Return Channel (ARC) technology.

The two devices are the same except where noted. SiI957n is used throughout this document to refer to both devices.

The SiI957n port processor offers an extensive set of audio features including audio extraction and insertion. Audio from the active HDMI input is sent to the main or subaudio output port. High-Bitrate (HBR) audio is supported on the main audio output port. Additionally, a 2-channel I^2S or an S/PDIF input receives PCM or bit stream audio from an audio DSP or a DTV SoC, and output to either the main or sub-HDMI output, or both.

The SiI957n port processor supports two independent ARC transceivers. Each ARC transceiver is configurable as an ARC receiver or transmitter. As an ARC receiver in an AVR or HTiB design, either the Tx0 or Tx1 HDMI output can receive an ARC signal from a DTV. As an ARC transmitter in a DTV design, the ARC signal can be transmitted out of the two of the six Rx HDMI inputs, which are designated as ARC-capable, to an AVR or soundbar.

The MHL to HDMI bridge function is available on two input ports; this allows consumers to attach their mobile devices to the AVR or DTV and view high definition content while the AVR or DTV charges the mobile device battery.

The SiI9575 device supports ViaPort Matrix Switch. While the main HDMI output selects one of the HDMI inputs, the second HDMI output can select another HDMI input or parallel video input. This is ideal for AVR Zone 2 support or PIP/POP function in DTV.

1.1. HDMI Inputs and Outputs

- Six HDMI input ports support 300 MHz simultaneously
- Two HDMI output ports that support 300 MHz simultaneously
- TMDS™ cores run up to 3.0 Gb/s
- HDMI, MHL, HDCP, and DVI compatible
- Supports video resolutions up to 4K × 2K @ 30 Hz, 8-bit, 1080p @ 60 Hz, 12-bit or 720p/1080i @ 120 Hz, 12-bit
- Supports 4K × 2K 50P/60P FPS when pixel format is $YC_b C_r$ 4:2:0.
- Supports all the mandatory and some optional 3D formats up to 300 MHz
- MHL support up to1080p @ 24 Hz on two input ports
- Pre-programmed with HDCP keys
- Repeater function supports up to 127 devices

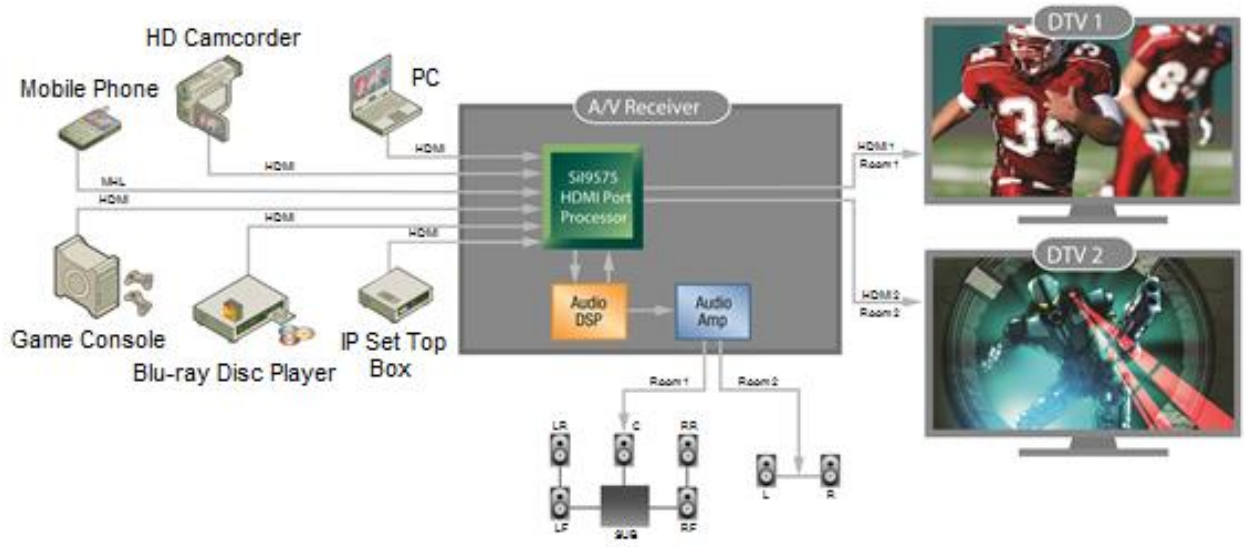


Figure 1.1. Port Processor Application

1.2. Performance Improvement Features

- InstaPort™ viewing technology reduces port switching time to less than one second
- InstaPrevue technology provides a picture-in-picture preview of connected source devices
- AVI, Audio InfoFrame, and video input resolution detection for all input ports, accessible port-by-port
- Hardware-based HDCP error detection and recovery minimizes firmware intervention
- Automatic output mute and unmute based on link stability, such as cable connect/detach

1.3. Audio Inputs and Outputs

- Two S/PDIF inputs and two S/PDIF outputs supporting PCM and compressed audio formats up to 192 kHz such as Dolby Digital, DTS, and AC-3
- DSD output supports Super Audio CD applications, up to 6 channels
- I^2S outputs support PCM, DVD-Audio output, up to 8-channel 192 kHz
- I^2S inputs support PCM, DVD-Audio input, up to 2-channel 192 kHz
- High-Bitrate audio output support such as DTS-HD MA and Dolby® TrueHD
- Sample Rate Converter (SRC) supports down sampling 2:1 and 4:1
- Two HDMI ARC inputs or outputs support

1.4. Control Capability

- Two independent Consumer Electronics Control (CEC) interfaces with HDMI-compliant CEC I/O to support two sink devices
- Integrated EDID in non-volatile memory and DDC support for the HDMI ports using separate 256-byte SRAM for the HDMI ports and 128-byte SRAM for VGA EDID
- Individual control of Hot Plug Detect (HPD) for each of the input ports
- Controllable by the local I^2C bus

1.5. Packaging

176-pin, 20 mm × 20 mm, 0.4 mm pitch TQFP package with an exposed pad (ePad)

2. Functional Description

Figure 2.1 shows the block diagram of the SiI957n port processor.

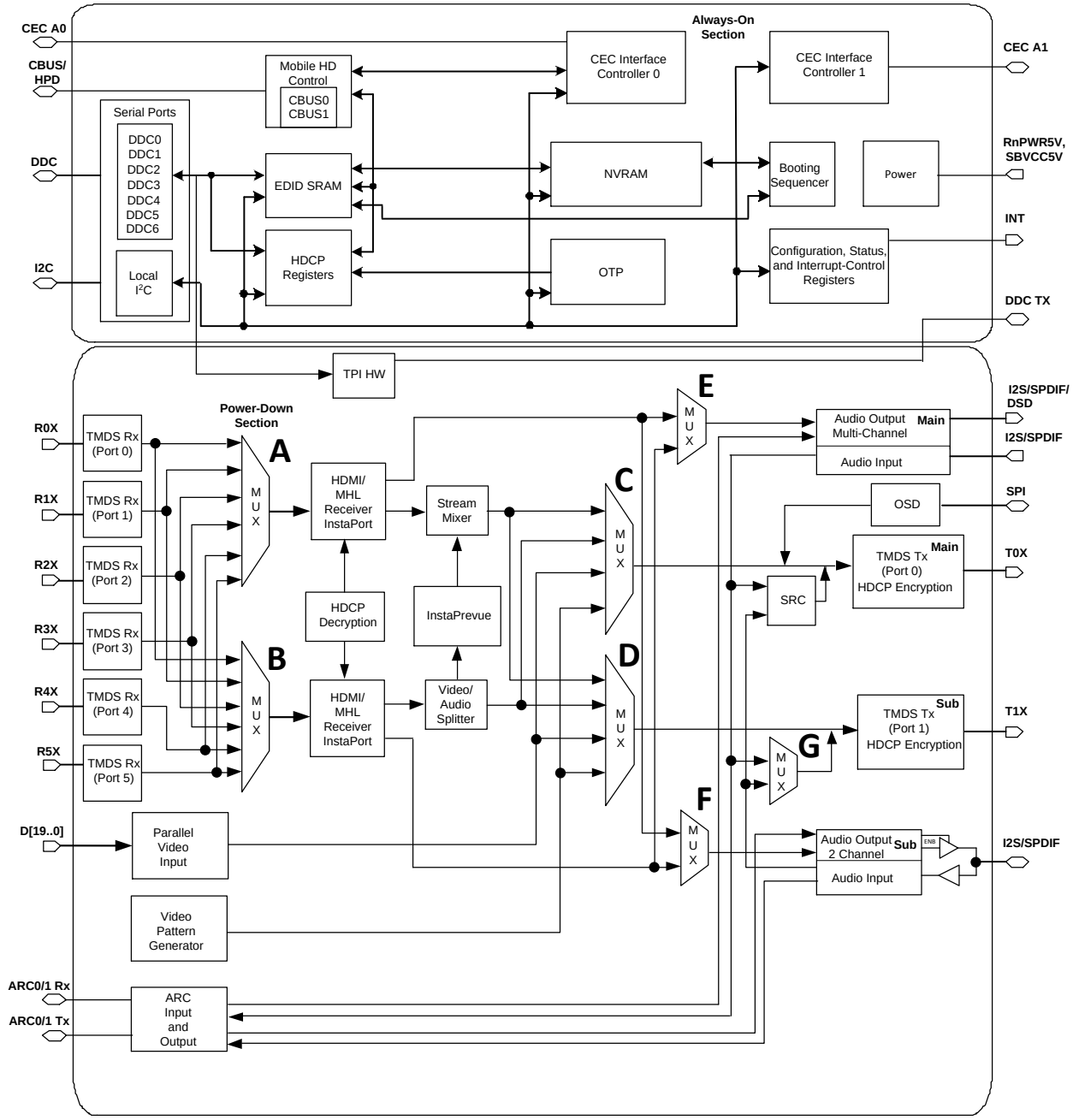


Figure 2.1. Functional Block Diagram

2.1. Always-on Section

The Always-on section contains the low speed control circuits of the HDMI connection, and includes the I^{2}C interfaces, internal memory blocks, and the registers that control the blocks of the Power-down section.

2.1.1. Serial Ports Block

The Serial Ports Block provides eight I^2C serial interfaces: six DDC ports to communicate with the HDMI or DVI hosts, one VGA DDC port, and one local I^2C port for initialization and control by a local microcontroller in the display or AVR. Each interface is 5 V tolerant. Figure 2.2 shows the connection of the local I^2C port to the system microcontroller.

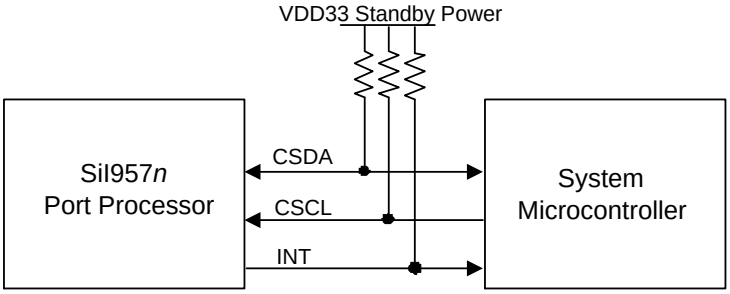


Figure 2.2. I^2C Control Configuration

The seven DDC interfaces (DDC 0–6) on the SiI957n port processor are slave interfaces that can run up to 400 kHz. Each interface connects to one E-DDC bus and is used to read the integrated EDID and HDCP authentication information. The port is accessible on the E-DDC bus at device addresses 0xA0 for the EDID and 0x74 for HDCP control. The transmitter DDC master controller supports accessing HDCP and EDID up to 100 kHz. Local I^2C can also access the transmitter DDC bus; in this case, an internal oscillator provides the clock source.

2.1.2. Static RAM Block

The Static RAM (SRAM) Block contains 2,560 bytes of RAM. Each port is allocated a 256-byte block for DDC; this allows all ports to be read simultaneously from six different sources connected to the SiI957n device. A 128-byte block is available for VGA DDC, 768 bytes are available for Key Selection Vectors (KSV), 64 bytes are used for the auto-boot feature, and 64 bytes are reserved. Every EDID and SHA KSV has an offset location. The SRAM can be written to and read from using the local I^2C interface and it can be read through the DDC interface. The memory can be read through the DDC interface without main TV power, using only 5 V power from the HDMI connector.

2.1.3. NVRAM Block

The port processor contains 512 bytes of NVRAM, 256 of which is used to store common EDID data used by each of the ports, 128 of which is used for VGA DDC, and 64 of which is used by the auto boot feature. 64 bytes are unused. Both the NVRAM EDID data and NVRAM auto-boot data should be initialized by software using the local I^2C bus at least once during the time of manufacture.

2.1.4. HDCP Registers Block

The HDCP Registers Block controls the necessary logic to decrypt the incoming audio and video data. The decryption process is controlled entirely by the host-side microcontroller using a set sequence of register reads and writes through the DDC channel. The decryption process uses preprogrammed HDCP keys and Key Selection Vector (KSV) stored in the on-chip nonvolatile memory.

2.1.5. OTP ROM Block

The Receiver One-Time Programmable (OTP) ROM Block is preprogrammed at the factory with HDCP keys. System manufacturers do not need to purchase key sets from Digital Content Protection, LLC. Lattice Semiconductor handles all purchasing, programming, and security for the HDCP keys. The preprogrammed HDCP keys provide the highest level of security possible, as it is not possible to read out the keys after they are programmed.

2.1.6. Booting Sequencer

The Booting Sequencer boots up the required data, such as EDID, initial HPD status, and MHL port selection from NVRAM during power on.

2.1.7. Configuration, Status, and Interrupt Control Block

The Configuration, Status, and Interrupt Control Registers Block incorporate the registers required for configuring and managing the features of the SiI957n port processor. These registers are grouped by functions such as RPI, TPI, CPI, MHL, and miscellaneous and are used to perform audio, video, and auxiliary format processing, HDMI 1.4a InfoFrame Packet format, and power-down control. The registers are accessible from the local I^2C port. This block also handles interrupt operation.

2.1.8. Mobile HD Control Block

The Mobile HD Control Block handles MHL DDC control. This block handles CBUS conversion to DDC signals for accessing the EDID and HDCP interface blocks.

2.1.9. CEC Interface Controller

Two independent Consumer Electronics Control (CEC) interface controllers are available in the SiI957n port processor. This gives the system designer the option to design a system that supports both primary CEC line and a secondary CEC line that are not physically connected to each other. For example, using an AVR featuring two DTV connections from the SiI957n device, the primary CEC line (CEC_A0 pin) can be connected to the CEC signal of all HDMI input ports of the AVR while the secondary CEC line (CEC_A1 pin) connects to the CEC signal of the second DTV.

Each CEC interface controller provides a CEC-compliant signal and has a high-level register interface accessible through the I^2C interface. Programming is done through the Lattice Semiconductor CEC Programming Interface (CPI). This controller makes CEC control easy and straightforward by removing the burden of requiring that the host processor perform these low-level transactions on the CEC bus. As a result, CEC pass-through mode is neither required nor supported.

The CEC controllers (CEC_A0 and CEC_A1) are identical except for the device address used to access them.

2.1.10. Power Block

The Power Block features an analog power multiplexer with inputs from the +5 V power from the R[0–5]PWR5V and the SBVCC5V sources. The output of the analog power multiplexer supplies power to the Always-On Section.

2.2. Power-down Section

The Power-down Section contains the HDMI high-speed data paths, including the analog TMDS input and output blocks and the digital logic for HDMI data and HDCP processing.

2.2.1. TMDS Receiver Blocks

The TMDS Receiver Blocks, defined as Port 0, Port 1, Port 2, Port 3, Port 4, and Port 5, are terminated separately, equalized under the control of the receiver digital block, and controlled by the local I^2C bus. Input data is over-sampled by five to enable the downstream DPLL block to capture the most stable signal at any given time.

2.2.2. 6:1 Input Multiplexer Blocks A and B and 4:1 Input Multiplexer Blocks C and D

6:1 Input Multiplexer Block A selects one of the six TMDS inputs and sends it to the main pipe. 6:1 Input Multiplexer Block B selects one of the six TMDS inputs and sends it to the subpipe. 4:1 Input Multiplexer Block C selects among main pipe, subpipe, parallel video, and video pattern generator sources and sends it to HDMI output Tx0. 4:1 Input Multiplexer Block D selects among main pipe, subpipe, parallel video, and video pattern generator sources and sends it to HDMI output Tx1. The specific function of the multiplexers is determined by whether InstaPort, InstaPrevue, or matrix switch mode is enabled.

In InstaPort or InstaPrevue modes, Multiplexer Block A selects the active input and sends it to the main pipe for processing. The subpipe functions as a roving pipe whereby Multiplexer Block B sequentially selects one of the five inactive inputs and sends it to the InstaPort or InstaPrevue blocks for processing. Multiplexer Blocks C and D can each independently select among main pipe, parallel video, and video pattern generator sources to send to HDMI output Tx0 and Tx1 respectively.

In matrix switch mode, Multiplexer Block A selects one active input and sends it to the main pipe for processing. roving is disabled and the subpipe functions as a second processing pipe for another active input selected by Multiplexer Block B. Multiplexer Blocks C and D can each independently select between main pipe and subpipe sources to send to HDMI output Tx0 and Tx1, respectively. Matrix Switch mode is supported on the SiI9575 device only.

2.2.3. HDMI, MHL, and InstaPort Receiver Blocks

The HDMI, MHL, and InstaPort Receiver blocks perform functions including deskewing, analyzing packets, processing the main pipe and roving pipe, multiplexing, demultiplexing, repeater functions, and HDCP authentication. The SiI957n device supports six HDMI input ports. MHL can be enabled on any two input ports selected at the time of manufacture by programming a register in the NVRAM.

2.2.4. Video/Audio Splitter Block

The Video/Audio Splitter Block separates the video and audio data from the TMDS stream for the roving pipe. The video is sent to the InstaPrevue block and the audio is sent to Multiplexer Blocks C and D. This can be used in the InstaPrevue Picture-In-Picture (PIP) mode in which a single sub-window is displayed on the main video. The audio from the sub-window can replace the audio from the main video before being sent to Tx0 and Tx1.

2.2.5. InstaPrevue Block

The InstaPrevue Block captures and processes all of the preauthenticated HDMI/DVI/MHL subframe images from the roving pipe. The operating preview mode is configured in this block.

2.2.6. Stream Mixer Block

The Stream Mixer Block replaces a region of the main port video with a sub-frame image from the InstaPrevue block. It merges sub-frames with the main video input at the proper screen locations specified by external software register settings.

2.2.7. 2:1 Input Multiplexer Blocks E and F and Main and Subaudio Formatting Blocks

2:1 Input Multiplexer Block E selects either the decoded audio stream from the TMDS input to main pipe or the subpipe and sends it to the main audio block to be processed as I^2S and S/PDIF. The main audio block supports 8-channel PCM and 6-channel DSD for I^2S and 2-channel PCM and compressed audio formats for S/PDIF. 2:1 Input Multiplexer Block F selects either the decoded audio stream from the TMDS input to main pipe or the subpipe and sends it to the subaudio block to be sent out as I^2S and S/PDIF. The subaudio block supports 2-channel PCM for I^2S and 2-channel PCM and compressed audio formats for S/PDIF.

2.2.8. Parallel Video Input Block

The Parallel Video Input Block features a 20-bit parallel video input interface which supports input clocks up to 165 MHz in dual edge and single edge modes. In dual edge mode, incoming data is latched on both edges of the clock for double data rate (DDR) to support up to 720p/1080i @ 60 Hz for RGB/YCbCr 4:4:4 formats. In single edge mode, incoming data is latched on one edge of the clock for single data rate (SDR) to support up to 1080p @ 60 Hz and UXGA @ 60 Hz for YCbCr 4:2:2 formats.

Video processing features support color space conversion, 4:2:2 to 4:4:4 up- and 4:4:4 to 4:2:2 down-sampling, RGB range expansion, RGB/YCbCr range compression, clipping, and dithering functions. All of these functions can be bypassed through register settings.

The color space conversion feature performs color conversion from YCbCr to RGB and RGB to YCbCr according to the selected color space standard ITU-R BT.601 for standard-definition DTV and ITU-R BT.709 for high-definition DTV.

Chrominance up-sampling increases the number of chrominance samples in each line of video. Up-sampling doubles the number of chrominance samples in each line, converting 4:2:2 sampled video to 4:4:4 sampled video.

Chrominance down-sampling decreases the number of chrominance samples in each line of video. Down-sampling halves the number of chrominance samples in each line, converting 4:4:4 sampled video to 4:2:2 sampled video.

The SiI957n port processor can scale the input color range from limited-range into full range using the range expansion block. When enabled by itself, the range expansion block expands 16–235 limited-range data into 0–255 full-range data for each video channel. When range expansion and the YCbCr to RGB color space converter are both enabled, the input conversion range for the Cb and Cr channels is 16–240.

When enabled by itself, the range compression block compresses 0–255 full range data into 16–235 limited range data for each video channel. When enabled with the RGB to YCbCr converter, this block compresses to 16–240 for the Cb and Cr channels. The color range scaling is linear.

When enabled, the clipping block clips the values of the output video to 16–235 for RGB video for the Y channel, and to 16–240 for the Cb and Cr channels.

The SiI957n port processor can dither the video by adding a pseudorandom number to every value. The 18-bit dithering result can be truncated or rounded. Additionally, dithering can be enabled or disabled by video component (R, G, B, Y, Cb, or Cr).

2.2.9. Video Pattern Generator Block

The Video Pattern Generator (VPG) Block supplies one of eight predefined video patterns to the HDMI transmitters. The predefined video patterns are solid red, solid green, solid blue, solid black, solid white, ramp, 8 × 6 chessboard, and color bars. The video patterns have an RGB color space at 480p, 576p, and 720p video resolutions.

An example use for the VPG is to combine the predefined video pattern with an external audio input to create a complete HDMI stream which can then be sent out of the HDMI transmitter to a sound bar. The VPG can also be used for test purposes during product development.

The VPG requires a pixel clock for its operation. One of several clock sources, including the crystal oscillator (xclk), audio VCO clock 0, or audio VCO clock 1, can be used to generate the pixel clock for the VPG. If the crystal oscillator (xclk), audio VCO clock 0, or audio VCO clock 1 is used as the clock source for the VPG, then the frequency of the external audio crystal must be 27 MHz to generate the correct pixel clock frequencies for the VPG. Incorrect pixel clock frequencies will be generated if the external audio crystal used is not 27 MHz; the range specified in Table 3.20 on page 23 will not work for this function. The xclk is generated from the external audio crystal. The audio VCO clock 0 is an output of a PLL which uses the xclk as the input. The audio VCO clock 1 is an output of another PLL which also uses the xclk as the input. Table 2.1 shows the pixel clock source and frequency for the VPG at 480p, 576p and 720p video resolutions. Refer to the Programmer's Reference for details on configuring the VPG.

Table 2.1. Pixel Clock Source and Frequency

Video Resolution	Pixel Clock Source	Pixel Clock Frequency
480p, 576p	xclk	27 MHz
720p	audio VCO clock 0 or audio VCO clock 1	(27 MHz) • (11/4) = 74.25 MHz

The audio VCO clock 0 and VCO clock 1 PLLs are shared with the audio extraction logic. Therefore, if audio VCO clock 0 or VCO clock 1 is used for the VPG, the respective main or subport audio extraction mode needs to be disabled.

2.2.10. Audio Sampling Rate Converter Block

The audio Sampling Rate Converter (SRC) Block allows the inserted 2-channel PCM audio from either the main- or sub-audio ports to be down-sampled before combining with the HDMI stream from the main pipe and sending to Tx0. The audio data can be down-sampled by a factor of 2 or 4 by register control. Conversions from: 192 kHz to 48 kHz, 176.4 kHz to 44.1 kHz, 96 kHz to 48 kHz, and 88.2 kHz to 44.1 kHz are supported.

2.2.11. On-screen Display Controller

The On-screen Display Controller (OSD) Block supports a text-based onscreen display that allows for up to four character-based windows to be overlaid onto the video displayed from the Tx0 HDMI output. The OSD supports three font sizes: 12×16, 16 × 24 and 24 × 32 pixels, to provide flexibility for choosing the character and icon size in the OSD windows.

OSD supports 480p, 576p, 720p, 1080p, and 1080iHDMI 2D video formats. OSD is supported on SiI957n Tx0 HDMI output only. OSD may be combined on the displayed video along with InstaPrevue windows to form a complete menu system.

A 12 kB on-chip RAM memory stores the OSD font bit maps and window index information. The OSD memory can be loaded by the host microcontroller through the I^2C bus or from an external flash memory though the Serial Peripheral Interface (SPI). The SPI supports clock frequencies of 1.6875 MHz, 3.375 MHz, 13.5 MHz, and 27 MHz. This interface is used to read and write the external flash memory. In addition, the host microcontroller can program the external flash memory using I^2C through the SPI interface.

2.2.12. Audio Input Block

The Audio Input Block supports external audio insertion into the transmitted HDMI streams. There are two audio input blocks: the main audio port and the subaudio port. The inserted audio to the main audio port is two-channel I^2S or a single S/PDIF. Similarly, the inserted audio to the subaudio port is two-channel I^2S or a single S/PDIF.

Both main audio port and subaudio port insertion support the following audio formats:

- I^2S: 2 channels
  - PCM: 2 channels
- S/PDIF: IEC 60958 and IEC 61937
  - PCM: 2channels
  - Compressed bit-stream: Dolby® Digital, Dolby Digital Plus, Dolby Digital EX, Dolby Digital Surround EX DTS, DTS ES

Each of the SiI957n I^2S main and subaudio port insertion requires SCK, WS, and SD0 signals for two channel I^2S. For both the main and subaudio ports, the SiI957n device supports CTS and N value generation without requiring an MCLK input.

The SiI957n main audio port S/PDIF insertion shares the same pin with SD0 of the I^2S insertion. The function of this pin is configured by software.

The SiI957n subaudio port S/PDIF insertion shares the same pin with SD0 of the I^2S insertion. The function of this pin is configured by software. In addition, the subaudio port I^2S and S/PDIF insertion pins are multiplexed with the subaudio port I^2S and S/PDIF extraction pins. The functions of these pins are configured by software.

The audio inserted into the main audio port can be combined with the HDMI stream from the main pipe and sent to Tx0 or combined with the HDMI stream from the subpipe and sent to Tx1. Similarly, the audio inserted to the subaudio port can be combined with the HDMI stream from the main pipe and sent to Tx0 or combined with the HDMI stream from the subpipe and sent to Tx1. The audio sampling rate converter block selects between inserted audio from the main audio port and the subaudio port to send to Tx0. Input Multiplexer G selects between inserted audio from the main audio port and the subaudio port to send to Tx1.

2.2.13. Audio Output Block

The Audio Output Block supports audio extraction from the received HDMI/MHL streams. There are two audio output blocks, the main audio port and the subaudio port. The extracted audio from the main audio port is eight-channel I2S, six-channel DSD, or a single S/PDIF audio. The extracted audio from the subaudio port is either two-channel I2S or single S/PDIF audio.

- Main Audio Port Extraction
  - I^2S: 8 channels
    PCM: up to 8 channels
    HBR: Dolby TrueHD, DTS-HD Master Audio
  - DSD: 6 channels
  - S/PDIF: IEC 60958 and IEC 61937
    PCM: 2 channels
    Compressed bit-stream: Dolby Digital, Dolby Digital Plus, Dolby Digital EX, Dolby Digital Surround EX, DTS, DTS-ES
- Subaudio Port Extraction
  - I^2S: 2 channels
    PCM: 2 channels
  - S/PDIF: IEC 60958 and IEC 61937
    PCM: 2 channels
    Compressed bit-stream: Dolby Digital, Dolby Digital Plus, Dolby Digital EX, Dolby Digital Surround EX, DTS, DTS-ES

By default, the main audio port is configured for eight-channel I^2S audio extraction from the main pipe and the subaudio port is configured for two-channel I^2S audio extraction from the subpipe. The SiI957n device allows swapping the main and subaudio ports to provide two-channel I^2S audio extraction from the main pipe and eight-channel I^2S audio extraction from the subpipe.

The SiI957n I^2S audio extraction provides the MCLK, SCK, WS, SD0, SD1, SD2, and SD3 signals for eight-channel I^2S from the main audio port and SCK, WS, and SD0 for two-channel I^2S for the subaudio port. To generate the MCLK for the subaudio port, an external PLL clock generator can be used.

The SiI957n main audio port I^2S, DSD, and S/PDIF audio extraction pins are shared. The functions of these pins are configured by software.

The SiI957n subaudio port S/PDIF audio extraction shares the same pin with SD0 of the I^2S audio extraction. The function of this pin is configured by software. In addition, the subaudio port I^2S and S/PDIF audio extraction pins are multiplexed with the subaudio port I^2S and S/PDIF audio insertion pins. The functions of these pins are configured by software.

2.2.14. Audio Return Channel (ARC) Input and Output

The Audio Return Channel (ARC) feature eliminates an extra cable when sending audio from an HDMI sink device to an adjacent HDMI source or repeater device. This is done by allowing a single IEC60958-1 or IEC61937 audio stream to travel in the opposite direction of the TMDS signal on its own conductor in the HDMI cable, after negotiation using CEC Audio Return Channel Control. The HDMI sink device implements the ARC transmitter and the HDMI source or repeater device implements the ARC receiver.

The SiI957n device provides two ARC transceiver channels. Each pin can be independently configured to operate as an ARC transmitter or an ARC receiver. For example, the SiI957n device designed into a DTV can use the ARC transmitter feature while the SiI957n device designed into an AVR can use the ARC receiver feature. For an ARC transmitter, the ARC transceiver pin is connected to the ARC pin of the connector for the HDMI Rx port that is designated as ARC-capable. For an ARC receiver, the ARC transceiver pin is connected to the ARC pin of the HDMI connector for the transmitter port that is designated as ARC-capable.

ARC transceivers can share pins with the HDMI Ethernet Channel (HEC) signals. The SiI957n device does not support HEC and therefore cannot use HEC and ARC simultaneously on the same receiver port.

The SiI957n device supports only single mode ARC. The SiI957n ARC receiver can be made compatible for common mode ARC by using an AC-coupling network between the HPD and NC pins of the HDMI connector of the transmitter port and the SiI957n ARC receiver pin.

2.2.15. TMDS Transmitter Block

The TMDS Transmitter Blocks perform HDCP encryption and 8-to-10-bit TMDS encoding on the data to be transmitted over the HDMI link. The encoded data is sent to the three TMDS differential data lines, along with a TMDS differential clock line. Internal source termination eliminates the need to use external R-C components for signal shaping. The internal source termination can be disabled by registers settings. The SiI957n port processor integrates two HDMI output ports, which enables zone-2 support by using the ViaPort Matrix Switch feature of the device. Both transmitter ports support up to 300 MHz.

3. Electrical Specifications

3.1. Absolute Maximum Conditions

Table 3.1. Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Notes
AVDD33	TMDS core supply voltage	−0.3	—	4.0	V	1, 2
IOVCC33	I/O supply voltage	−0.3	—	4.0	V	1, 2
SBVCC5	5 V standby power supply voltage	−0.3	—	5.7	V	1, 2
R[0–5]PWR5V	5 V input from power pin of HDMI connector	−0.3	—	5.7	V	1, 2
XTALVCC33	PLL crystal oscillator power	−0.3	—	4.0	V	1, 2
AVDD13	TMDS receiver core supply voltage	−0.3	—	1.5	V	1, 2
APLL13	PLL Analog VCC	−0.3	—	1.5	V	1, 2
CVCC13	Digital core supply voltage	−0.3	—	1.5	V	1, 2
TDVDD13	TMDS transmitter core supply voltage	−0.3	—	1.5	V	1, 2
TPVDD13	TMDS transmitter core supply voltage	−0.3	—	1.5	V	1, 2
V_I	Input voltage	−0.3	—	IOVCC33 + 0.3	V	1, 2
V_O	Output voltage	−0.3	—	IOVCC33 + 0.3	V	1, 2
T_J	Junction temperature	0	—	125	°C	—
T_{STG}	Storage temperature	−65	—	150	°C	—

Notes:

1. Permanent damage can occur to the device if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described in the Normal Operating Conditions section below.

3.2. Normal Operating Conditions

Table 3.2. Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Notes
AVDD33	TMDS core supply voltage	3.14	3.3	3.46	V	—
IOVCC33	I/O supply voltage	3.14	3.3	3.46	V	—
SBVCC5	5 V standby power supply voltage	4.5	5.0	5.5	V	1
R[0–5]PWR5V	5 V input from power pin of HDMI connector	4.5	5.0	5.5	V	—
XTALVCC33	PLL crystal oscillator power	3.14	3.3	3.46	V	—
AVDD13	TMDS receiver core supply voltage	1.25	1.3	1.35	V	2
APLL13	PLL Analog VCC	1.25	1.3	1.35	V	2
CVCC13	Digital core supply voltage	1.25	1.3	1.35	V	2
TDVDD13	TMDS transmitter core supply voltage	1.25	1.3	1.35	V	2
TPVDD13	TMDS transmitter core supply voltage	1.25	1.3	1.35	V	2
AVDD13	TMDS receiver core supply voltage	1.27	1.3	1.35	V	3
APLL13	PLL Analog VCC	1.27	1.3	1.35	V	3
CVCC13	Digital core supply voltage	1.27	1.3	1.35	V	3
TDVDD13	TMDS transmitter core supply voltage	1.27	1.3	1.35	V	3
TPVDD13	TMDS transmitter core supply voltage	1.27	1.3	1.35	V	3
T_A	Ambient temperature (with power applied)	0	+25	+70	°C	—
Θ_{ja}	Ambient thermal resistance (Theta JA)	—	22.0	—	°C/W	—
Θ_{jc}	Junction to case resistance (Theta JC)	—	—	6.0	°C/W	—

Notes:

1. SBVCC5 voltage is measured at SBVCC5TP as shown in Figure 3.1.
2. For 4 HDMI Inputs and 2 HDMI output running simultaneously at 300MHz
3. For 5 or 6 HDMI Inputs and 2 HDMI Outputs running simultaneously at 300MHz

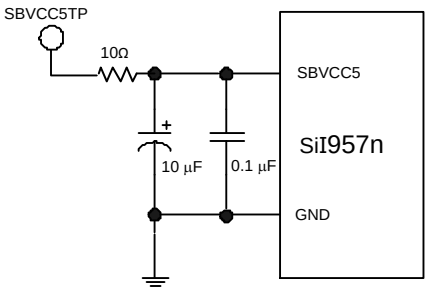


Figure 3.1. Test Point SBVCC5TP for SBVCC5 Measurement

3.3. DC Specifications

Table 3.3. Digital I/O DC Specifications

Symbol	Parameter	Pin Type	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level Input Voltage	LVTTL	—	2.0	—	—	V
V_{IL}	LOW-level Input Voltage	LVTTL	—	—	—	0.8	V
V_{TH+DDC}	LOW-to-HIGH Threshold, DDC Buses	Schmitt	—	3.0	—	—	V
V_{TH-DDC}	HIGH-to-LOW Threshold, DDC Buses	Schmitt	—	—	—	1.5	V
V_{TH+I2C}	LOW-to-HIGH Threshold, I^2C Buses	Schmitt	—	2.0	—	—	V
V_{TH-I2C}	HIGH-to-LOW Threshold, I^2C Buses	Schmitt	—	—	—	0.8	V
V_{OH}	HIGH-level Output Voltage	LVTTL	—	2.4	—	—	V
V_{OL}	LOW-level Output Voltage	LVTTL	—	—	—	0.4	V
I_{OL}	Output Leakage Current	—	High Impedance	−10	—	10	µA
I_{OD4}	4 mA Digital Output Drive	LVTTL	V_{OUT} = 2.4 V	4	—	—	mA
			V_{OUT} = 0.4 V	4	—	—	mA
$V_{TH+RESET}$	LOW-to-HIGH Threshold, Reset	Schmitt	—	2.0	—	—	V
$V_{TH-RESET}$	HIGH-to-LOW Threshold, Reset	Schmitt	—	—	—	0.8	V
V_{CINL}	Input Clamp Voltage	All	—	—	—	GND –0.3	V
V_{CIPL}	Input Clamp Voltage	All	—	—	—	IOVCC33 +0.3	V

Table 3.4. TMDS Input DC Specifications – HDMI Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{ID}	Differential Mode Input Voltage	—	150	—	1200	mV
V_{ICM}	Common Mode Input Voltage	—	AVDD33 –400	—	AVDD33 –37.5	mV

Table 3.5. TMDS Input DC Specifications – MHL Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IDC}	Single-ended Input DC Voltage	—	AVDD33 –1200	—	AVDD33 –300	mV
V_{IDF}	Differential Mode Input Swing Voltage	—	200	—	1000	mV
V_{ICM}	Common Mode Input Swing Voltage	—	170	—	Min (720, 0.85 V_{IDF})	mV

Table 3.6. TMDS Output DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
V_{SWING}	Single-ended Output Swing Voltage	R_{LOAD} = 50 Ω	400	—	600	mV	—
V_H	Single-ended High-level Output Voltage	—	AVDD33 –200	—	AVDD33 +10	mV	—
V_L	Single-ended Low-level Output Voltage	—	AVDD33 –700	—	AVDD33 –400	mV	—
$V_{TH+RSEN}$	LOW-to-HIGH Threshold, RSEN	—	0.8	—	1.1	V	1
$V_{TH-RSEN}$	HIGH-to-LOW Threshold, RSEN	—	0.3	—	0.5	V	2

Notes:

4. RSEN deasserted state to asserted state threshold voltage when sink Rx termination transitions from disabled to enabled.
5. RSEN asserted state to deasserted state threshold voltage when sink Rx termination transitions from enabled to disabled.

Table 3.7. Single Mode Audio Return Channel DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{el}	Operating DC Voltage	—	0	—	5	V
$V_{el\ swing}$	Swing Amplitude	—	400	—	600	mV

Table 3.8. S/PDIF Input Port DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
Z_{I_SPDIF}	Termination Impedance	—	—	75	—	Ω	1
		—	—	4	—	kΩ	2
V_{I_SPDIF}	Input Voltage	75 Ω termination, AC-coupled	400	—	600	mV_{PP}	3

Notes:

1. This impedance is implemented with an external 75 Ω resistor to ground and is used when the interconnection is over a 75 Ω COAX cable.
2. This is the internal impedance of the S/PDIF input.
3. The S/PDIF input can also be safely driven at LVTTL voltage levels without AC coupling. The 75 Ω termination is not required in this case.

Table 3.9. CEC DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH+CEC}	LOW to HIGH Threshold	—	2.0	—	—	V
V_{TH-CEC}	HIGH to LOW Threshold	—	—	—	0.8	V
V_{OH_CEC}	HIGH-level Output Voltage	—	2.5	—	—	V
V_{OL_CEC}	LOW-level Output Voltage	—	—	—	0.6	V
I_{IL_CEC}	Input Leakage Current	Power Off; R*n*PWR5V = 0 V	—	—	1.8	µA

Table 3.10. CBUS DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH_CBUS}	High-level Input Voltage	—	1.0	—	—	V
V_{IL_CBUS}	Low-level Input Voltage	—	—	—	0.6	V
V_{OH_CBUS}	High-level Output Voltage	I_{OH} = 100 µA	1.5	—	1.9	V
V_{OL_CBUS}	Low-level Output Voltage	I_{OL} = –100 µA	—	—	0.2	V
Z_{DSC_CBUS}	Pull-down Resistance – Discovery	—	800	1000	1200	Ω
Z_{ON_CBUS}	Pull-down Resistance – Active	—	90	100	110	kΩ
I_{IL_CBUS}	Input Leakage Current	High Impedance	—	—	1	µA
C_{CBUS}	Capacitance	Power On	—	—	80	pF

Table 3.11. Power

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{APLL13}	Supply Current for APLL13	—	—	3	mA	1
I_{AVDD13}	Supply Current for AVDD13	—	—	250	mA	1
I_{AVDD33}	Supply Current for AVDD33	—	—	345	mA	1
$I_{IOVCC33}$	Supply Current for IOVCC33	—	—	2	mA	1
$I_{XTALVCC33}$	Supply Current for XTALVCC33	—	—	<1	mA	1
I_{CVCC13}	Supply Current for CVCC13	—	—	680	mA	1
$I_{SBVCC5STBY}$	Supply Current for SBVCC5 in Standby mode	—	—	8	mA	2
$I_{SBVCC5ACT}$	Supply Current for SBVCC5 in Active mode	—	—	30	mA	1
$I_{TDVDD13}$	Supply Current for TDVDD13	—	—	60	mA	1
$I_{TPVDD13}$	Supply Current for TPVDD13	—	—	30	mA	1
Total	Total Power	—	—	2.6	W	1

Notes:

1. With six 300 MHz HDMI receiver inputs with InstaPort, InstaPrevue, audio outputs, and OSD on and two 300 MHz transmitter outputs.
2. With no active AV sources connected to the HDMI Rx inputs.

3.4. AC Specifications

Table 3.12. TMDS Input Timing AC Specifications – HDMI Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{RXDPS}	Intrapair Differential Input Skew	—	—	—	0.4	T_{BIT}
T_{RXCCS}	Channel-to-Channel Differential Input Skew	—	—	—	$0.2T_{PIXEL}$ + 1.78	ns
F_{RXC}	Differential Input Clock Frequency	—	25	—	300	MHz
T_{RXC}	Differential Input Clock Period	—	3.33	—	40	ns
T_{IJIT}	Differential Input Clock Jitter Tolerance (0.3Tbit)	300 MHz	—	—	100	ps

Table 3.13. TMDS Input Timing AC Specifications – MHL Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{SKEW_DF}	Input Differential Intrapair Skew	—	—	—	93	ps
T_{SKEW_CM}	Input Common-mode Intrapair Skew	—	—	—	93	ps
F_{RXC}	Differential Input Clock Frequency	—	25	—	75	MHz
T_{RXC}	Differential Input Clock Period	—	13.33	—	40	ns
T_{CLOCK_JIT}	Common Mode Clock Jitter Tolerance	—	—	—	$0.3T_{BIT}$ + 266.7	ps
T_{DATA_JIT}	Differential Data Jitter Tolerance	—	—	—	$0.4T_{BIT}$ + 88.88	ps

Table 3.14. TMDS Output Timing AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{TXDPS}	Intrapair Differential Output Skew	—	—	—	0.15	T_{BIT}
T_{TXRT}	Data/Clock Rise Time	20%–80%	75	—	—	ps
T_{TXFT}	Data/Clock Fall Time	80%–20%	75	—	—	ps
F_{TXC}	Differential Output Clock Frequency	—	25	—	300	MHz
T_{TXC}	Differential Output Clock Period	—	3.33	—	40	ns
T_{DUTY}	Differential Output Clock Duty Cycle	—	40%	—	60%	T_{TXC}
T_{OJIT}	Differential Output Clock Jitter	—	—	—	0.25	T_{BIT}

Table 3.15. Single Mode Audio Return Channel AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{ASMRT}	Rise Time	10%–90%	—	—	60	ns
T_{ASMFT}	Fall Time	90%–10%	—	—	60	ns
T_{ASMJIT}	Jitter Max	—	—	—	0.05	UI*
F_{ASMDEV}	Clock Frequency Deviation	—	–1000	—	1000	ppm

***Note:** Proportional to unit time (UI), according to sample rate. Refer to the S/PDIF specification.

Table 3.16. CEC AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{R_CEC}	Rise Time	10%–90%	—	—	250	µs
T_{F_CEC}	Fall Time	90%–10%	—	—	50	µs

Table 3.17. CBUS AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{BIT_CBUS}	Bit Time	1 MHz clock	0.8	—	1.2	µs
T_{BJIT_CBUS}	Bit-to-Bit Jitter	—	–1%	—	+1%	T_{BIT_CBUS}
T_{DUTY_CBUS}	Duty Cycle of 1 Bit	—	40%	—	60%	T_{BIT_CBUS}
T_{R_CBUS}	Rise Time	0.2 V–1.5 V	5	—	200	ns
T_{F_CBUS}	Fall Time	0.2 V–1.5 V	5	—	200	ns
ΔT_{RF}	Rise-to-Fall Time Difference	—	—	—	100	ns

Table 3.18. Video Input Timing AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{CIP}	IDCK Period, One Pixel per Clock	—	6.06	—	40	ns	—	1
F_{CIP}	IDCK Frequency, One Pixel per Clock	—	25	—	165	MHz	—	1
T_{CIP12}	IDCK Period, Dual-edge Clock	—	12.12	—	40	ns	—	2
F_{CIP12}	IDCK Frequency, Dual-edge Clock	—	25	—	82.5	MHz	—	2
T_{DUTY}	IDCK Duty cycle, One Pixel per Clock	—	40%	—	60%	T_{CIP}	Figure 4.1	—
T_{DUTY12}	IDCK Duty Cycle, Dual-edge Clock	—	45%	—	55%	T_{CIP12}	Figure 4.1	—
T_{IJIT}	Worst Case IDCK Clock Jitter	—	—	—	1.0	ns	—	3, 4
T_{SIDF}	Setup Time to IDCK Falling Edge	EDGE = 0	1.0	—	—	ns	Figure 4.3	5
T_{HIDF}	Hold Time to IDCK Falling Edge		2.2	—	—	ns		
T_{SIDR}	Setup Time to IDCK Rising Edge	EDGE = 1	1.0	—	—	ns	Figure 4.2	5
T_{HIDR}	Hold Time to IDCK Rising Edge		2.2	—	—	ns		
T_{SIDD}	Setup Time to IDCK Rising or Falling Edge	Dual-edge Clocking	1.0	—	—	ns	Figure 4.4	6
T_{HIDD}	Hold Time to IDCK Rising or Falling Edge		2.2	—	—	ns		

Notes:

1. TCIP and FCIP apply in single-edge clocking modes. TCIP is the inverse of FCIP and is not a controlling specification.
2. TCIP12 and FCIP12 apply in dual-edge mode. TCIP12 is the inverse of FCIP12 and is not a controlling specification.
3. Input clock jitter is estimated by triggering a digital scope at the rising edge of the input clock, and measuring peak-to-peak time spread of the rising edge of the input clock 1 microsecond after the triggering.
4. Actual jitter tolerance can be higher depending on the frequency of the jitter.
5. Setup and hold time specifications apply to Data, DE, VSYNC, and HSYNC input pins, relative to IDCK input clock.
6. Setup and hold limits are not affected by the setting of the EDGE bit for 8/10/12-bit dual-edge clocking mode.

3.4.1. Control Signal Timing Specifications

Under normal operating conditions unless otherwise specified.

Table 3.19. Control Signal Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
T_{RESET}	RESET# signal LOW time required for reset	—	50	—	—	µs	1, 5
T_{I2CDVD}	SDA Data Valid Delay from SCL falling edge on READ command	CL = 400pF	—	—	700	ns	2, 6
$t_{SU;DAT}$	I^2C data setup time	—	210	—	—	ns	7
T_{HDDAT}	I^2C data hold time	0–400 kHz	2.0	—	—	ns	3, 6
T_{INT}	Response time for INT output pin from change in input condition (HPD, Receiver Sense, VSYNC change, etc.).	RESET# = HIGH	—	—	100	µs	—
F_{SCL}	Frequency on master DDC SCL signal	—	40	70	100	kHz	4
F_{CSCL}	Frequency on master CSCL signal	—	40	—	400	kHz	—

Notes:

1. Reset on RESET# signal can be LOW as the supply becomes stable (shown in Figure 4.5), or pulled LOW for at least T_{RESET} (shown in Figure 4.6).
2. All standard-mode (100 kHz) I^2C timing requirements are guaranteed by design. These timings apply to the slave I^2C port (pins CSDA and CSCL) and to the master I^2C port (pins DSDA and DSCL).
3. This minimum hold time is required by CSCL and CSDA signals as an I^2C slave. The device does not include the 300 ns internal delay required by the I^2C Specification (Version 2.1, Table 5, note 2).
4. The master DDC block provides an SCL signal for the E-DDC bus. The HDMI Specification limits this to I^2C Standard Mode or 100 kHz. Use of the Master DDC block does not require an active IDCK.
5. Not a Schmitt trigger.
6. Operation of I^2C pins above 100 kHz is defined by LVTTL levels V_{IH}, V_{IL}, V_{OH}, and V_{OL}. For these levels, I^2C speeds up to 400 kHz (fast mode) are supported.
7. In default configuration, operation at 400 kHz does not meet the $t_{SU;DAT}$ data setup time required by the I^2C Specification. For advanced configuration information, refer to SiI-PR-1054 revision D or later.

Table 3.20. Audio Crystal Frequency

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{XTAL}	External Crystal Frequency	—	26	27	28.5	MHz

Note: F_{xtal} must be 27 MHz if the crystal oscillator (xclk) is used as the clock source for the Video Pattern Generator.

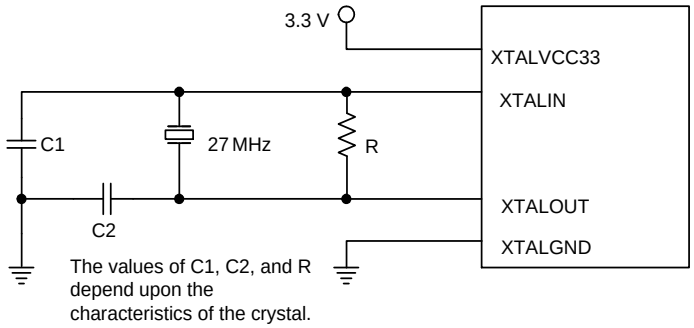


Figure 3.2. Audio Crystal Schematic

Note: The XTALIN/XTALOUT pin pair must be driven with a clock in all applications.

3.4.2. Audio Input Timing

Table 3.21. S/PDIF Input Port AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
F_{S_SPDIF}	Sample Rate	2 Channel	32	—	192	kHz	—	—
T_{SPCYC}	S/PDIF Cycle Time	C_L = 10 pF	—	—	1.0	UI	Figure 4.10	1
T_{SPDUTY}	S/PDIF Duty Cycle	C_L = 10 pF	90%	—	110%	UI	Figure 4.10	1

Note: Refer to the notes for Table 3.22.

Table 3.22. I^2S Input Port AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
F_{S_I2S}	Sample Rate	—	32	—	192	kHz	—	—
T_{SCKCYC}	I^2S Cycle Time	CL = 10 pF	—	—	1.0	UI	Figure 4.9	1
$T_{SCKDUTY}$	I^2S Duty Cycle	CL = 10 pF	90%	—	110%	UI	Figure 4.9	—
T_{I2SSU}	I^2S Setup Time	CL = 10 pF	15	—	—	ns	Figure 4.9	2
T_{I2SHD}	I^2S Hold Time	CL = 10 pF	0	—	—	ns	Figure 4.9	2

Notes:

1. Proportional to unit time (UI) according to sample rate. Refer to the I^2S or S/PDIF specifications.
2. Setup and hold minimum times are based on 13.388 MHz sampling, which is adapted from Figure 3 of the Philips I^2S Specification.

3.4.3. Audio Output Timing

Table 3.23. I^2S Output Port AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{TR}	SCK Clock Period (TX)	C_L = 10 pF	1.0	—	—	T_{TR}
T_{HC}	SCK Clock HIGH Time	C_L = 10 pF	0.35	—	—	T_{TR}
T_{LC}	SCK Clock LOW Time	C_L = 10 pF	0.35	—	—	T_{TR}
T_{SU}	Setup Time, SCK to SD/WS	C_L = 10 pF	$0.4T_{TR} - 5$	—	—	ns
T_{HD}	Hold Time, SCK to SD/WS	C_L = 10 pF	$0.4T_{TR} - 5$	—	—	ns
$T_{SCKDUTY}$	SCK Duty Cycle	C_L = 10 pF	40	—	60	% T_{TR}
T_{SCK2SD}	SCK to SD or WS Delay	C_L = 10 pF	–5.0	—	5.0	ns

Note: Refer to Figure 4.11 on page 29.

Table 3.24. S/PDIF Output Port AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{SPCYC}	SPDIF Cycle Time	C_L = 10 pF	—	1.0	—	UI[1]
F_{SPDIF}	SPDIF Frequency	—	4.0	—	24.0	MHz
T_{SPDUTY}	SPDIF Duty Cycle	C_L = 10 pF	90.0	—	110.0	% T_{SPCYC}
$T_{MCLKCYC}$	MCLK Cycle Time	C_L = 10 pF	20.0	—	250	ns
F_{MCLK}	MCLK Frequency	C_L = 10 pF	4.0	—	50.0	MHz
$T_{MCLKDUTY}$	MCLK Duty Cycle	C_L = 10 pF	45	—	65	% $T_{MCLKCYC}$

Notes:

1. Proportional to unit time (UI), according to sample rate. Refer to the S/PDIF specification.
2. Refer to Figure 4.12 on page 29 and Figure 4.13 on page 29.

3.5. Serial Flash SPI Interface AC Specifications

Table 3.25. Serial Flash AC Specifications

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCLK}	Clock Frequency	1.6875	—	27	MHz
T_{SCLKH}	Clock HIGH Time	16	—	—	ns
T_{SCLKL}	Clock LOW Time	16	—	—	ns
T_{SLCH}	SS Active Setup Time	11	—	—	ns
T_{CHSH}	SS Not Active Hold Time	11	—	—	ns
T_{DVCH}	SDI Data Out Setup Time	6	—	—	ns
T_{CHDX}	SDI Data Out Hold Time	6	—	—	ns
T_{CLQV}	Clock LOW-to-SDO Data In Valid	—	—	16	ns

Note: Refer to Figure 4.14 on page 30.

4. Timing Diagrams

4.1. Video Input Timing Diagrams

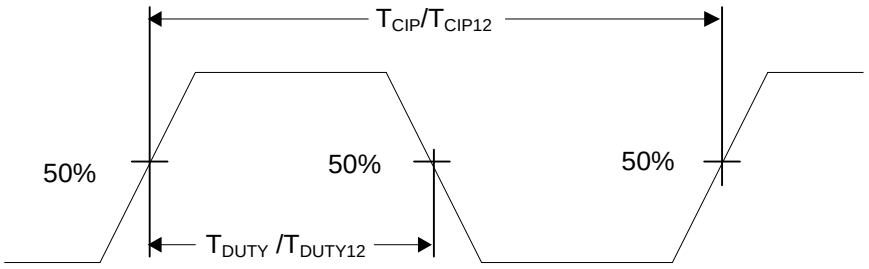
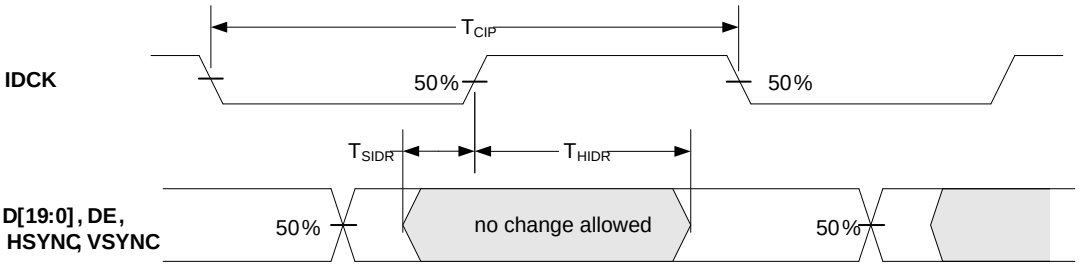
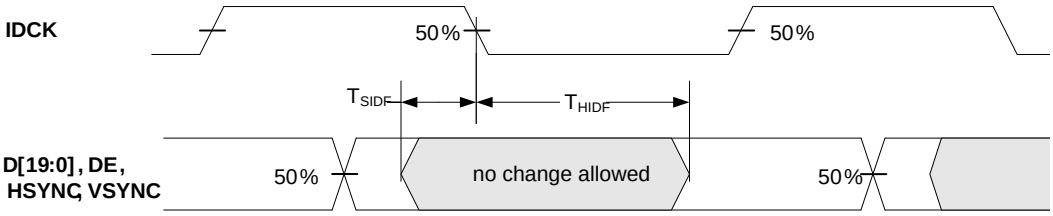


Figure 4.1. IDCK Clock Duty Cycle



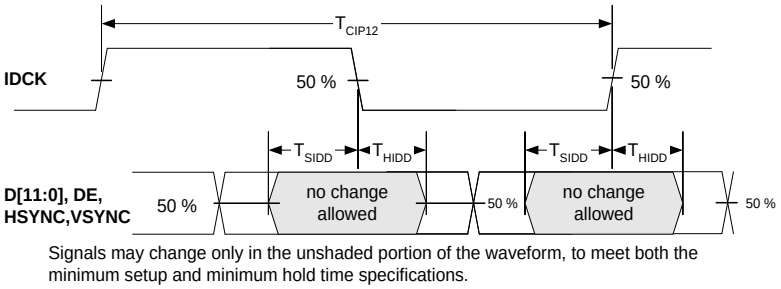
Signals may change only in the unshaded portion of the waveform to meet both the minimum setup and minimum hold time specifications

Figure 4.2. Control and Data Single-Edge Setup and Hold Times—EDGE = 1



Signals may change only in the unshaded portion of the waveform to meet both the minimum setup and minimum hold time specifications

Figure 4.3. Control and Data Single-Edge Setup and Hold Times—EDGE = 0



Signals may change only in the unshaded portion of the waveform, to meet both the minimum setup and minimum hold time specifications.

Figure 4.4. Control and Data Dual-Edge Setup and Hold Times

4.2. Reset Timing Diagrams

VCC must be stable between the limits shown in the Normal Operating Conditions section on page 18 for T_{RESET} before RESET# goes HIGH, as shown in Figure 4.5. Before accessing registers, RESET# must be pulled LOW for T_{RESET}. This can be done by holding RESET# LOW until T_{RESET} after stable power, or by pulling RESET# LOW from a HIGH state for at least T_{RESET}, as shown in Figure 4.6. Note: VCC can be one of R*n*PPWR5V or SBVCC5V.

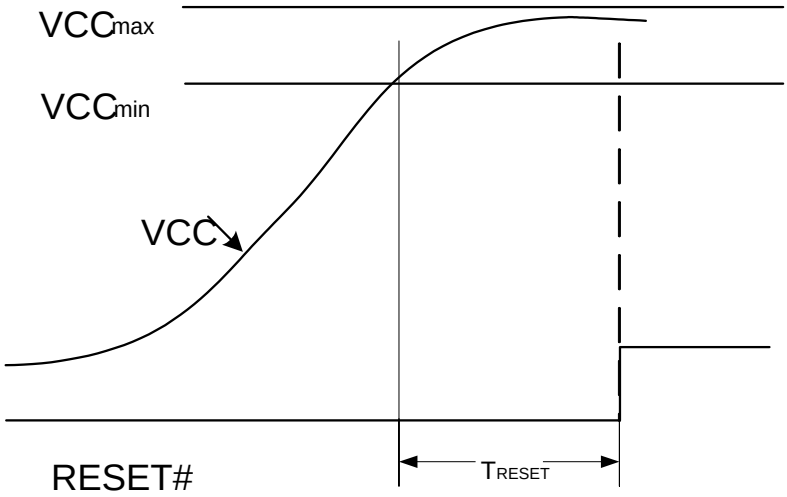


Figure 4.5. Conditions for Use of RESET#

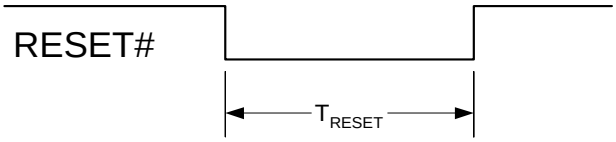


Figure 4.6. RESET# Minimum Timing

4.3. I²C Timing Diagrams

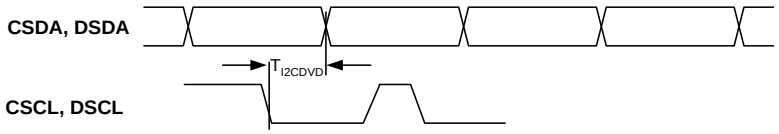


Figure 4.7. I²C Data Valid Delay (Driving Read Cycle Data)

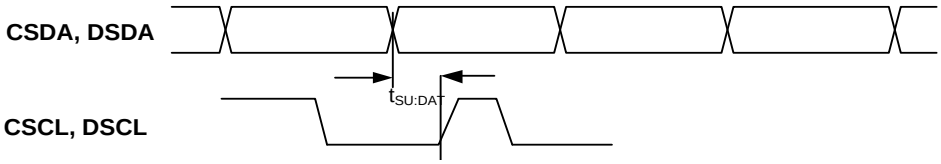


Figure 4.8. I²C Data Setup Time

4.4. Digital Audio Input Timing

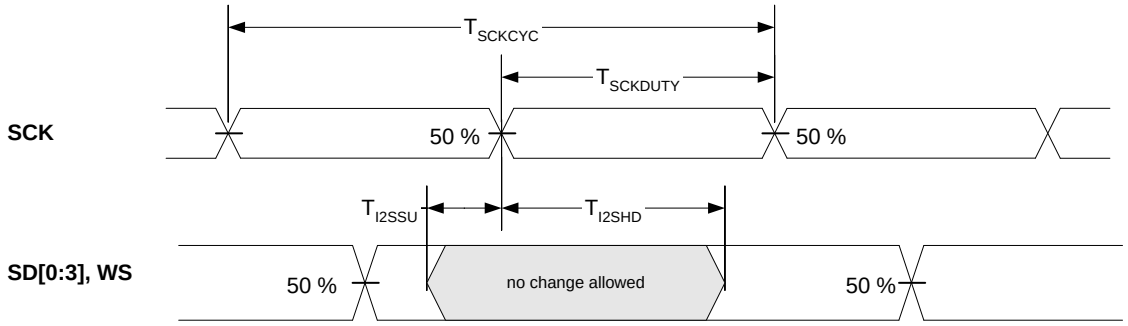


Figure 4.9. I²S Input Timing

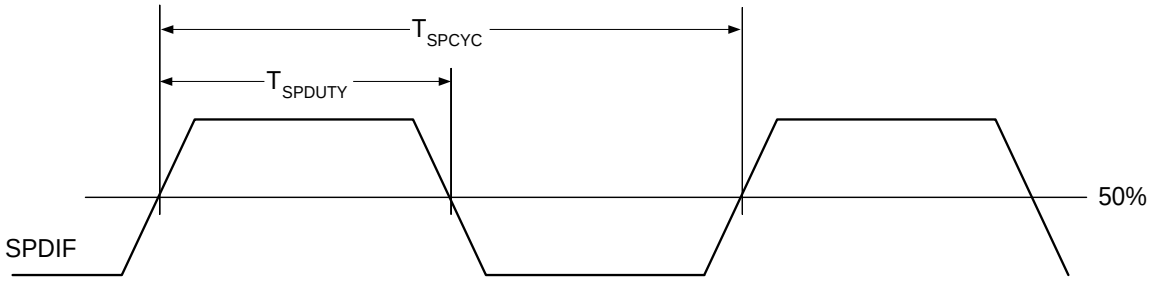


Figure 4.10. S/PDIF Input Timing

4.5. Digital Audio Output Timing

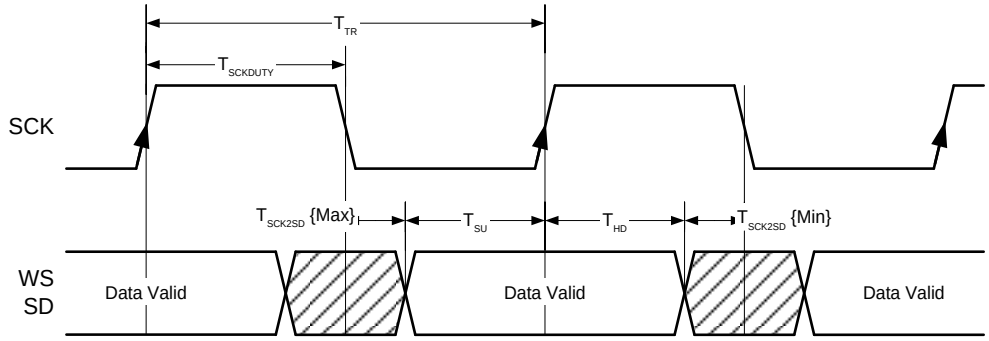


Figure 4.11. I²S Output Timing

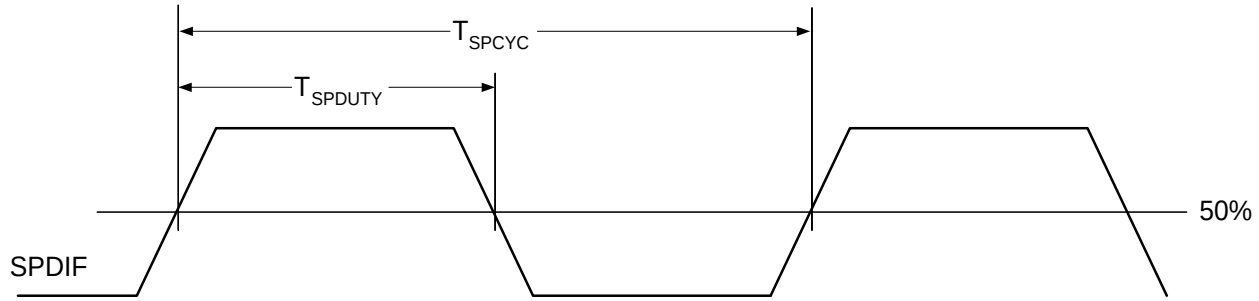


Figure 4.12. S/PDIF Output Timing

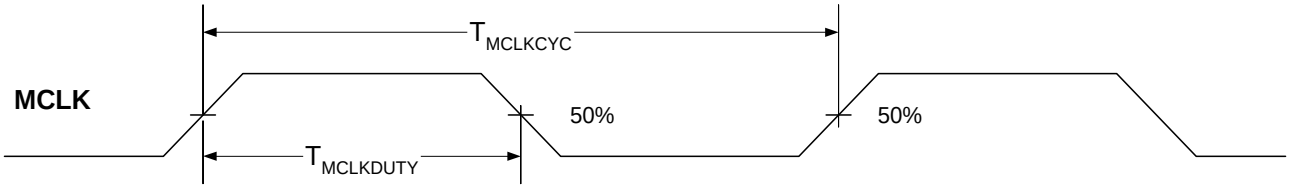


Figure 4.13. MCLK Timing

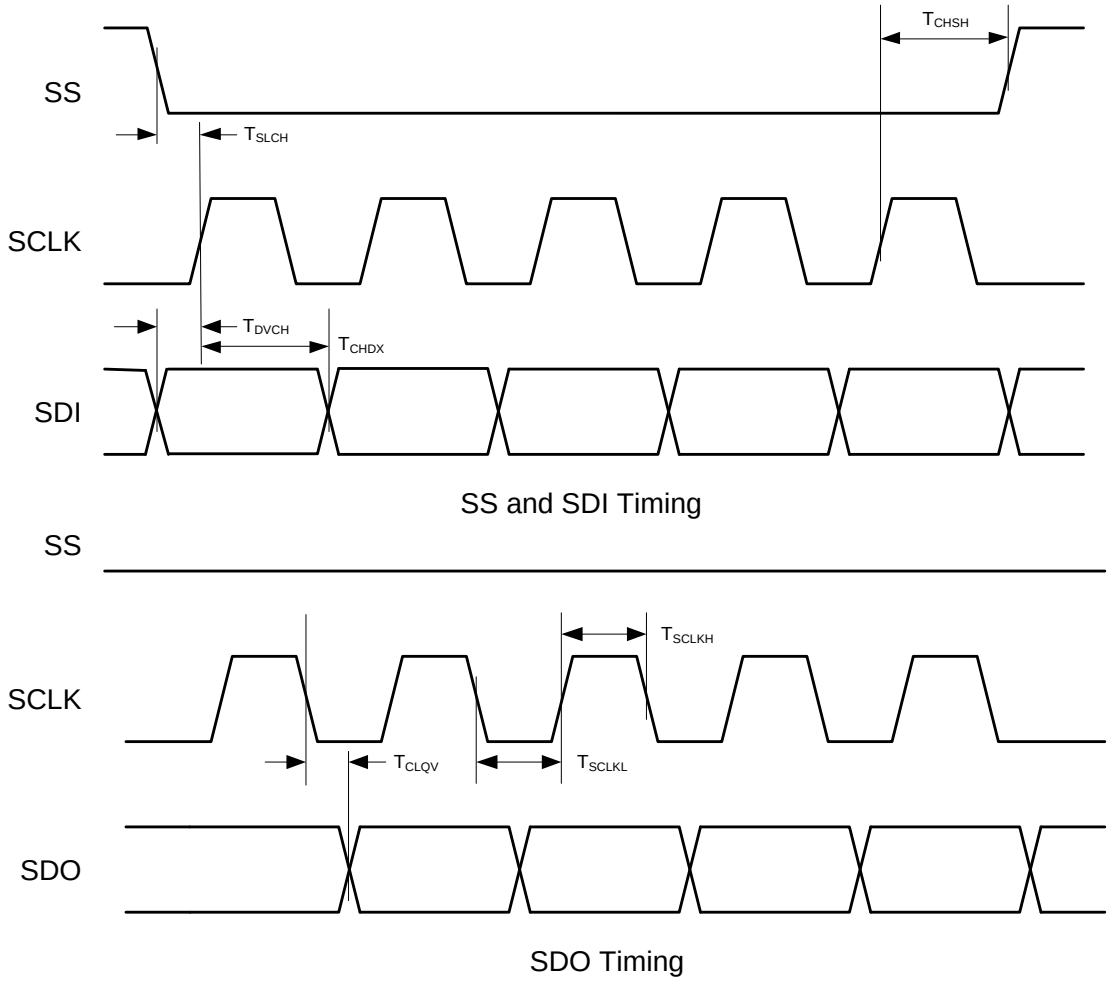


Figure 4.14. SPI Flash Memory Timing

5. Pin Diagram and Pin Descriptions

5.1. Pin Diagram

Figure 5.1 shows the pin assignments of the SiI957n port processor. Individual pin functions are described in the Pin Descriptions section on the next page. The package is a 20 × 20 × 0.4 mm 176-pin TQFP with an ePad, which ***must*** be connected to ground.

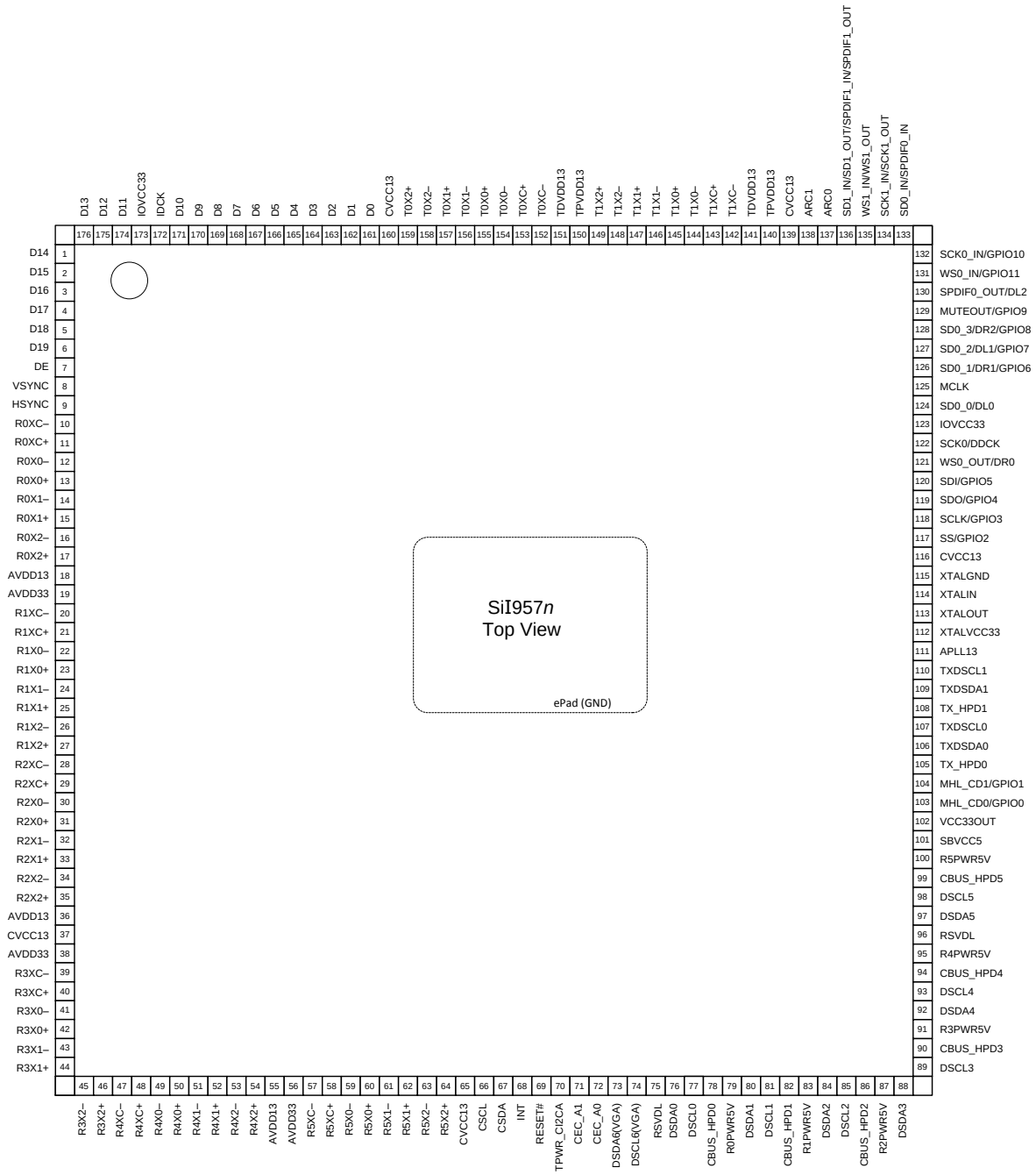


Figure 5.1. Pin Diagram (Top View)

5.2. Pin Descriptions

5.2.1. HDMI Receiver and MHL Port Pins

Name	Pin	Type	Dir	Description
R0X0+	13	TMDS	Input	HDMI Receiver Port 0 TMDS Input Data Pairs.
R0X0–	12			
R0X1+	15			
R0X1–	14			
R0X2+	17			
R0X2–	16			
R0XC+	11	TMDS	Input	HDMI Receiver Port 0 TMDS Input Clock Pair.
R0XC–	10			
R1X0+	23	TMDS	Input	HDMI Receiver Port 1TMDS Input Data Pairs.
R1X0–	22			
R1X1+	25			
R1X1–	24			
R1X2+	27			
R1X2–	26			
R1XC+	21	TMDS	Input	HDMI Receiver Port 1 TMDS Input Clock Pair.
R1XC–	20			
R2X0+	31	TMDS	Input	HDMI Receiver Port 2 TMDS Input Data Pairs.
R2X0–	30			
R2X1+	33			
R2X1–	32			
R2X2+	35			
R2X2–	34			
R2XC+	29	TMDS	Input	HDMI Receiver Port 2 TMDS Input Clock Pair.
R2XC–	28			
R3X0+	42	TMDS	Input	HDMI Receiver Port 3 TMDS Input Data Pairs.
R3X0–	41			
R3X1+	44			
R3X1–	43			
R3X2+	46			
R3X2–	45			
R3XC+	40	TMDS	Input	HDMI Receiver Port 3 TMDS Input Clock Pair.
R3XC–	39			
R4X0+	50	TMDS	Input	HDMI Receiver Port 4 TMDS Input Data Pairs.
R4X0–	49			
R4X1+	52			
R4X1–	51			
R4X2+	54			
R4X2–	53			
R4XC+	48	TMDS	Input	HDMI Receiver Port 4 TMDS Input Clock Pair.
R4XC–	47			

5.2.2. HDMI Receiver and MHL Port Pins *(continued)*

Name	Pin	Type	Dir	Description
R5X0+	60	TMDS	Input	HDMI Receiver Port 5 TMDS Input Data Pairs.
R5X0–	59			
R5X1+	62			
R5X1–	61			
R5X2+	64			
R5X2–	63			
R5XC+	58	TMDS	Input	HDMI Receiver Port 5 TMDS Input Clock Pair.
R5XC–	57			

Note: For Port *n* and Port *m* that have been configured as MHL inputs, the R*n*X0+ and R*n*X0– pin pair and R*m*X0+ and R*m*X0– pin pair carry the respective MHL signals.

5.2.3. HDMI Transmitter Port Pins

Name	Pin	Type	Dir	Description
T0X0+	155	TMDS	Output	HDMI Transmitter Port 0 TMDS Output Data Pairs. Main HDMI transmitter output port TMDS data pairs.
T0X0–	154			
T0X1+	157			
T0X1–	156			
T0X2+	159			
T0X2–	158			
T0XC+	153	TMDS	Output	HDMI Transmitter Port 0 TMDS Output Clock Pair. Main HDMI transmitter output port TMDS clock pair.
T0XC–	152			
T1X0+	145	TMDS	Output	HDMI Transmitter Port 1 TMDS Output Data Pairs. Sub-HDMI transmitter output port TMDS data pairs.
T1X0–	144			
T1X1+	147			
T1X1–	146			
T1X2+	149			
T1X2–	148			
T1XC+	143	TMDS	Output	HDMI Transmitter Port 1 TMDS Output Clock Pair. Sub-HDMI transmitter output port TMDS clock pair.
T1XC–	142			

5.2.4. Audio Return Channel Pins

Name	Pin	Type	Dir	Description
ARC0	137	Analog	Input/ Output	Audio Return Channels 0 and 1. These pins are used to transmit or receive an IEC60958-1 audio stream. In ARC transmitter mode, received on the SPDIF*n*_IN input pin, this pin transmits an S/PDIF signal to an ARC receiver-capable source (such as HTiB) or a repeater (such as AVR) devices, using single-mode ARC. In ARC receiver mode, transmitted through the SPDIF*n*_OUT pin, this pin receives an S/PDIF signal from an ARC transmitter-capable sink (such as DTV) device, using single-mode ARC. In combination with external components, common-mode ARC can be received. Each channel can either be an ARC input or an ARC output at one time.
ARC1	138			

5.2.5. Audio Pins

Name	Pin	Type	Dir	Description
MCLK	125	LVTTL	Output	Master Clock Output
SCK0/ DDCK	122	LVTTL	Output	Main Port I^2S Serial Clock Output/DSD Clock Output.
WS0_OUT/ DR0	121	LVTTL	Output	Main Port I^2S Word Select Output/DSD Data Right Bit 0.
SD0_0/ DL0	124	LVTTL	Output	Main Port I^2S Serial Data 0 Output/DSD Data Left Bit 0 Output.
SD0_1/DR1/ GPIO6	126	LVTTL	Output	Main Port I^2S Serial Data 1 Output/DSD Data Right Bit 1 Output/ Programmable GPIO 6.
SD0_2/DL1/ GPIO7	127	LVTTL	Output	Main Port I^2S Serial Data 2 Output/DSD Data Left Bit 1 Output/ Programmable GPIO 7.
SD0_3/DR2/ GPIO8	128	LVTTL	Output	Main Port I^2S Serial Data 3 Output/DSD Data Right Bit 2/ Programmable GPIO 8.
SPDIF0_OUT/ DL2	130	Analog/ LVTTL	Output	Main Port S/PDIF Output/DSD Data Left Bit 2.
SCK0_IN/ GPIO10	132	LVTTL	Input/ Output	Main Port I^2S Serial Clock Input/Programmable GPIO 10.
WS0_IN/ GPIO11	131	LVTTL	Input/ Output	Main Port I^2S Word Select Input/Programmable GPIO 11.
SD0_IN/ SPDIF0_IN	133	Analog/ LVTTL	Input	Main Port I^2S Serial Data Input/S/PDIF Input.
SCK1_IN/ SCK1_OUT	134	LVTTL	Input/ Output	Subport I^2S Serial Clock1 Input/I^2S Serial bit Clock Output.
WS1_IN/ WS1_OUT	135	LVTTL	Input/ Output	Subport I^2S Word Select Input/I^2S Word Select Output.
SD1_IN/ SD1_OUT/ SPDIF1_IN/ SPDIF1_OUT	136	LVTTL	Input/ Output	Subport I^2S Serial Data Input/I^2S Serial Data1 Output/ SPDIF Input//SPDIF Output.
MUTEOUT/ GPIO9	129	LVTTL	Input/ Output	Mute Audio Output/Programmable GPIO 9.

5.2.6. Crystal Pins

Name	Pin	Type	Dir	Description
XTALOUT	113	LVTTL 5 V tolerant	Output	Crystal clock output.
XTALIN	114	LVTTL 5 V tolerant	Input	Crystal clock input.

5.2.7. SPI Interface Pins

Name	Pin	Type	Dir	Description
SS/ GPIO2	117	LVTTL	Input/ Output	SPI Slave Select/Programmable GPIO 2.
SCLK/ GPIO3	118	LVTTL Schmitt Open-drain\	Input/ Output	SPI Clock/Programmable GPIO 3.
SDO/ GPIO4	119	LVTTL Schmitt Open-drain	Input/ Output	SPI Slave Data Output/Master Data Input/Programmable GPIO 4.
SDI/ GPIO5	120	LVTTL Schmitt Open-drain	Input/ Output	SPI Slave Data Input/Master Data Output/Programmable GPIO 5.

5.2.8. Parallel Video Bus

Name	Pin	Type	Dir	Description
D0	161	LVTTL	Input	Video Data Inputs. The video data inputs can be configured to support a wide variety of input formats, including multiple RGB and YCbCr bus formats, using register settings.
D1	162			
D2	163			
D3	164			
D4	165			
D5	166			
D6	167			
D7	168			
D8	169			
D9	170			
D10	171			
D11	174			
D12	175			
D13	176			
D14	1			
D15	2			
D16	3			
D17	4			
D18	5			
D19	6			
DE	7	LVTTL	Input	Data Enable Input
HSYNC	9	LVTTL	Input	Horizontal Sync Input
VSYNC	8	LVTTL	Input	Vertical Sync Input
IDCK	172	LVTTL	Input	Input Data Clock

5.2.9. DDC I²C Pins

Name	Pin	Type	Dir	Description
DSDA0	76	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	DDC I²C Data for respective HDMI receiver port. These signals are true open drain, and do not pull to ground when power is not applied to the device. These pins require an external pull-up resistor.
DSDA1	80			
DSDA2	84			
DSDA3	88			
DSDA4	92			
DSDA5	97			
DSDA6(VGA)	73	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	DDC I²C data for VGA port. This signal is true open drain, and does not pull to ground when power is not applied to the device. This pin requires an external pull-up resistor.
DSCL0	77	LVTTL Schmitt Open-drain 5 V tolerant	Input	DDC I²C Clock for respective HDMI receiver port. These signals are true open drain, and do not pull to ground when power is not applied to the device. These pins require an external pull-up resistor.
DSCL1	81			
DSCL2	85			
DSCL3	89			
DSCL4	93			
DSCL5	98			
DSCL6(VGA)	74	LVTTL Schmitt Open-drain 5 V tolerant	Input	DDC I²C Clock for VGA port. This signal is true open drain, and does not pull to ground when power is not applied to the device. This pin requires an external pull-up resistor.
TXDSDA0	106	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	DDC Master I²C Data for HDMI transmitter Port 0. This signal is true open drain, and does not pull to ground when power is not applied to the device. This pin requires an external pull-up resistor.
TXDSDA1	109	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	DDC Master I²C Data for HDMI transmitter Port 1. This signal is true open drain, and does not pull to ground when power is not applied to the device. This pin requires an external pull-up resistor.
TXDSCL0	107	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	DDC Master I²C Clock for HDMI transmitter Port 0. This signal is true open drain, and does not pull to ground when power is not applied to the device. This pin requires an external pull-up resistor.
TXDSCL1	110	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	DDC Master I²C Clock for HDMI transmitter Port 1 This signal is true open drain, and does not pull to ground when power is not applied to the device. This pin requires an external pull-up resistor.

5.2.10. Control Pins

Name	Pin	Type	Dir	Description
CSCL	66	Schmitt Open-drain 5 V tolerant	Input	Local Configuration/Status I^2C Clock. Chip configuration/status is accessed via this I^2C port. This pin is true open drain, so it does not pull to ground if power is not applied. See Figure 2.2 on page 10.
CSDA	67	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	Local Configuration/Status I^2C Data. Chip configuration/status is accessed via this I^2C port. This pin is true open drain, so it does not pull to ground if power is not applied. See Figure 2.2 on page 10.
RESET#	69	Schmitt	Input	External reset. Active LOW. Must be pulled up to VCC33OUT. When main power is not provided to the system, the microcontroller must present a high impedance of at least 100 kΩ to RESET#. If this condition is not met, a circuit to block the leakage from VCC33OUT to the microcontroller GPIO may be required.

5.2.11. System Switching Pins

Name	Pin	Type	Dir	Description
R0PWR5V	79	Power	Input	5 V Port detection input for respective HDMI receiver port. Connect to 5 V signal from HDMI input connector. These pins require a 10 Ω series resistor, a 5.1 kΩ pull down resistor, and at least a 1 µF capacitor to ground.
R1PWR5V	83			
R2PWR5V	87			
R3PWR5V	91			
R4PWR5V	95			
R5PWR5V	100			
CBUS_HPD0	78	LVTTL 1.5 mA 5 V tolerant Analog	Input/ Output	Hot Plug Detect output for the respective HDMI receiver port. In MHL mode, these pins serve as the respective CTRL bus.
CBUS_HPD1	82			
CBUS_HPD2	86			
CBUS_HPD3	90			
CBUS_HPD4	94			
CBUS_HPD5	99			
TX_HPD0	105	LVTTL 5 V tolerant	Input	Hot Plug Detect Input for HDMI transmitter Port 0.
TX_HPD1	108	LVTTL 5 V tolerant	Input	Hot Plug Detect Input for HDMI transmitter Port 1.
MHL_CD0/ GPIO0	103	LVTTL	Input/ Output	MHL Cable Detect 0/Programmable GPIO 0. MHL_CD0 is 5 V tolerant if SBVCC5 or one of the R[0-5]PWR5V is applied to the device. If none of these power supplies are applied, then MHL_CD0 is 3.3 V tolerant.
MHL_CD1/ GPIO1	104	LVTTL	Input/ Output	MHL Cable Detect 1/Programmable GPIO 1. MHL_CD1 is 5 V tolerant if SBVCC5 or one of the R[0-5]PWR5V is applied to the device. If none of these power supplies are applied, then MHL_CD1 is 3.3 V tolerant.

5.2.12. Configuration Pins

Name	Pin	Type	Dir	Description
TPWR_CI2CA	70	LVTTL	Input/ Output	I^2C Slave Address Input/Transmit Power Sense Output. During power-on-reset (POR), this pin is used as an input to latch the I^2C sub-address. The level on this pin is latched when the POR transitions from the asserted state to the de-asserted state. After completion of POR, this pin is used as the TPWR output. A register setting can change this pin to show if the active port is receiving a TMDS clock.
INT	68	Schmitt Open-drain 8 mA 3.3 V tolerant	Output	Interrupt Output. This is an open-drain output and requires an external pull-up resistor. This output can be safely pulled up to 3.3 V with no power (no SBVCC5, no R[0-5]PWR5V, no 3.3 V, and no 1.3 V) applied to the device.

5.2.13. CEC Pins

Name	Pin	Type	Dir	Description
CEC_A0	72	CEC Compliant 5 V tolerant, Schmitt triggered, LVTTL	Input/ Output	Primary CEC I/O used for interfacing to CEC devices This signal is electrically compliant with the CEC specification. As an input, this pin acts as an LVTTL Schmitt triggered input and is 5 V tolerant. As an output, the pin acts as an NMOS driver with resistive pull-up. This pin has an internal pull-up resistor. This signal should be connected to the CEC signal of all HDMI input and output ports if the system supports just one CEC line. ***OR*** In a system designed to have separate CEC connectivity for the HDMI input and output ports, this signal should be connected to the CEC signal of all the input ports supported in the system. This signal and CEC_A0 each connect to a separate CEC controller within the port processor and are independent of each other.
CEC_A1	71	CEC Compliant 5 V tolerant, Schmitt triggered, LVTTL	Input/ Output	Secondary CEC I/O used for interfacing to CEC devices. This signal is electrically compliant with the CEC specification. As an input, this pin acts as an LVTTL Schmitt triggered input and is 5 V tolerant. As an output, the pin acts as an NMOS driver with resistive pull-up. This pin has an internal pull-up resistor. This is an optional CEC signal provided for system designers who want to implement a system with two independent CEC lines, such as a system that supports a separate CEC line for the HDMI input ports and the HDMI output ports. In the example of a DTV that provides a second HDMI output using the SiI957n port processor; this signal can be connected to the CEC signal of the output port while the CEC_A1 signal is connected to the CEC signal of the input ports. This signal and CEC_A1 each connect to a separate CEC controller within the port processor and are independent of each other.

5.2.14. Power and Ground Pins

Name	Pin	Type	Description	Supply
AVDD33	19, 38, 56	Power	TMDS Core VDD. AVDD33 should be isolated from other system supplies to prevent leakage from the source device through the TMDS input pins. AVDD33 should not be used to power other system components that can be adversely affected by such leakage.	3.3 V
IOVCC33	123, 173	Power	I/O VCC.	3.3 V
SBVCC5	101	Power	Local Power from system. This pin requires a 10 Ω series resistor.	5.0 V
AVDD13	18, 36, 55	Power	TMDS Receiver Core VDD.	1.3 V
CVCC13	37, 65, 116, 139, 160	Power	Digital Core VCC.	1.3 V
APLL13	111	Power	PLL Analog VCC.	1.3 V
VCC33OUT	102	Power	Internal regulator 3.3 V output. VCC33OUT should not be used as a power source to provide power to other external circuits	3.3 V
TPVDD13	140, 150	Power	Analog Power for TMDS Tx core.	1.3 V
TDVDD13	141, 151	Power	Digital Power for TMDS Tx core.	1.3 V
XTALVCC33	112	Power	PLL crystal oscillator power.	3.3 V
XTALGND	115	Ground	PLL crystal oscillator ground.	GND
GND	ePad	Ground	The ePad ***must*** be soldered to ground, as this is the only ground connection for the device.	GND

5.2.15. Reserved Pin

Name	Pin	Type	Description
RSVDL	75	Reserved	Reserved, must be tied to ground.
RSVDL	96	Reserved	Reserved, must be tied to ground through a 4.7 kΩ pull-down resistor.

6. Feature Information

6.1. Standby and HDMI Port Power Supplies

The port processor has a 5-volt standby power supply pin (SBVCC5V) that can be used to supply power to the EDID and CEC portions of the device when all other power supplies are turned off. This arrangement results in a low-power mode, but allows the EDID to be readable and the CEC controllers to be operational. Table 6.1 summarizes the power modes available in the SiI957n port processor. Figure 6.1 shows a block diagram of the standby power supply sources and the always-on power island.

Table 6.1. Description of Power Modes

Power Mode	Description	SBVCC5	R*n*PWR5V	AVDD33	AVDD13
Power-on Mode	All power supplies to the SiI957n chip are on. All functions are available. The standby power supply is 5 V.	5 V	NA	3.3 V	1.3 V
Standby Power mode	The always-on power domain is on, supplied from the internal power MUX; all other supplies are off. The standby power supply is 5 V. In this mode, EDID and CEC are functional, but video and audio processing is not performed and all outputs are off.	5 V	NA	Off	Off
HDMI Port-only Power	Power is off to the device. HDMI +5 V from the HDMI cable is the only power source. For example, if the TV is unplugged from AC wall outlet, the EDID and CEC are functional in this mode.	Off	5 V on any input	Off	Off

Note: All other supplies are on in the power-on mode and off in all other modes.

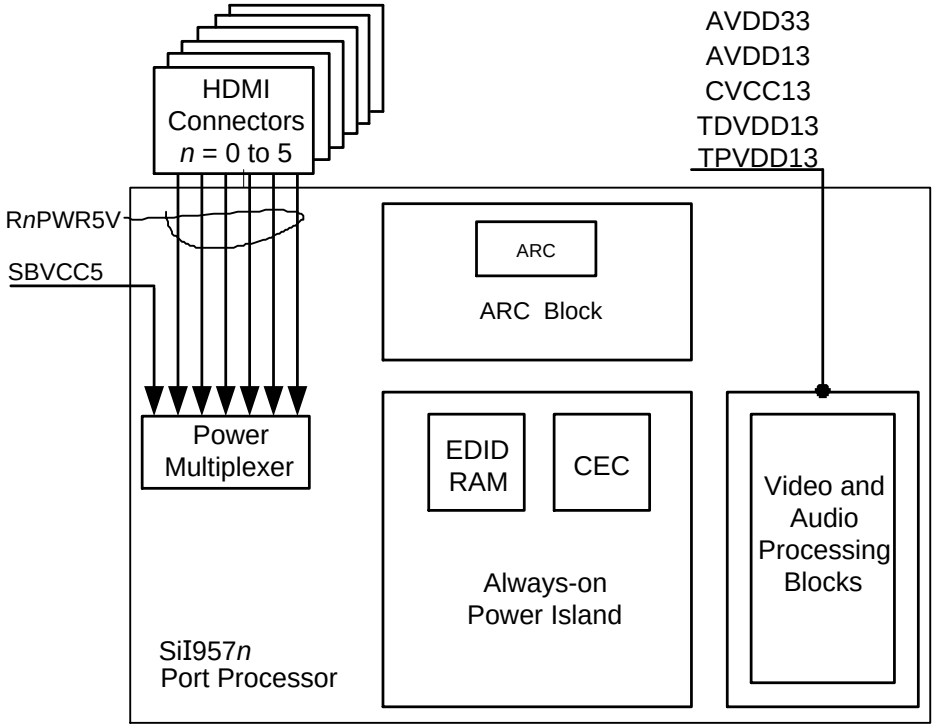


Figure 6.1. Standby Power Supply Diagram

If all power is off to the device, such as if the AVR or TV is unplugged from the AC electrical outlet, the EDID can still be read from the source by using power from the HDMI connector +5 V signal. In this case, the internal power MUX automatically switches to the HDMI connector power for powering the always-on logic. In this mode, only the EDID and CEC blocks are functional; all other functions of the device are in power-off mode. No damage will occur to the device in this mode.

6.2. InstaPort

The SiI957n port processor supports the InstaPort™ HDCP preauthentication feature, which hides the HDCP authentication time from the user. HDCP authentication is started on an upstream (input) port immediately after a source device is connected, regardless of whether the port is currently selected for output to the downstream sink device. All nonselected ports are HDCP authenticated in this manner and when HDCP is authenticated, it is maintained in the background. When a nonselected port is then selected, the authenticated content is immediately available because it does not have to reauthenticate HDCP. This InstaPort HDCP preauthentication feature reduces port switching times to less than one second.

6.3. InstaPrevue

The SiI957n device incorporates the InstaPrevue feature, which provides periodically updated picture-in-picture previews of each connected source device. The contents of each preauthenticated TMDS source device not being viewed can be displayed as a small subwindow overlaid onto the main video currently being viewed. With this feature, DTV and AVR manufacturers can provide the end-user with a content based, rather than a text based user interface for changing or selecting among various Blu-ray disc players, set-top boxes, DVD players, game consoles, or other HDMI/DVI/MHL connected sources.

InstaPrevue operates in one of three modes:

- The *All Preview* mode displays one to five sub-windows, selected by the user, regardless of whether a source device is connected or not. A subwindow with a manufacturer defined color is displayed for an unconnected source device.
- The *Active* mode displays only the subwindows for which there is a connected, active, and authenticated source device.
- The *Selected* mode displays a single subwindow for a connected source device selected by the user and is intended as a Picture-In-Picture (PIP) type preview.

InstaPrevue can be displayed on both Tx0 and Tx1 outputs of the SiI957n device. On the SiI9575 device, InstaPrevue does not operate in ViaPort Matrix Switch mode.

The supported combinations of main video display and InstaPrevue window formats are shown in the following table. InstaPrevue is compatible with RGB, YC4:4:4, and YC4:2:2 color formats.

Table 6.2. Supported InstaPrevue Window Formats

Main Video Display Format	InstaPrevue Window Format	Supported?
All supported 2D Resolutions	All supported 2D Resolutions except 4K×2K	Yes
	720p and 1080p 3D Frame Packing	Yes
	480p and 1080i 3D Frame Packing	No
	3D Side-by-Side (Half)	No
	3D Side-by-Side (Full)	No
	3D Top & Bottom	No
720p and 1080p 3D Frame Packing	All supported 2D Resolutions except 4K×2K	Yes
	720p and 1080p 3D Frame Packing	Yes
	480p and 1080i 3D Frame Packing	No
	3D Side-by-Side (Half)	No
	3D Top & Bottom	No
480p and 1080i 3D Frame Packing	All Formats	No
3D Top & Bottom		
3D Side-by-Side (Half)		
3D Side-by-Side (Full)		
4K×2K	All Formats	No

6.4. Support for UltraHD resolution at 50P/60P frames per second

The SiI957n device support 4K × 2K 50P and 4K × 2K 60p frame per second when pixel format is YC_bC_r 4:2:0 with TMDS clock frequency of 300 MHz. When configuring this mode, On-screen Display (OSD) and InstaPrevue must be disabled by the Firmware.

6.5. ViaPort Matrix Switch

The ViaPort Matrix Switch feature is available only on the SiI9575 device. When enabled, a different input source is sent to each of the two HDMI transmitter ports. The available input sources for the ViaPort Matrix Switch are any one of six TMDS input ports, an external parallel video input port, and an internal video pattern generator. This feature allows the system designer to implement a two zone system in an AVR or similar device.

6.6. MHL Receiver

The SiI957n port processor supports the Mobile High-definition Link (MHL) as a sink device on two of the six RX receiver ports selected at the time of manufacture. MHL is a high-speed multimedia data transfer protocol intended for use between mobile and display devices. The SiI957n device supports HDMI and MHL modes on the two selected RX receiver ports simultaneously. When an HDMI source is connected, the receiver port is configured as an HDMI port. When an MHL source is connected, an MHL cable detect sense signal from the cable is asserted and sent to the SiI957n device and also to the host microcontroller as an interrupt to configure the receiver port as an MHL port and to initiate the CBUS discovery process.

MHL carries video, audio, auxiliary, control data, and power across a cable consisting of five conductors. One connection is for a dedicated ground which is used as the 0V reference for the signals on the remaining four connections. Two other conductors form a single channel TMDS differential signal pair used to send video, audio and auxiliary data from the source device to the sink device. On the SiI957n device, the MHL TMDS channel differential signal pair pins are shared with the RX0+ and RX0– pins of the HDMI TMDS channel differential signal pair. Another connection is for the MHL Control Bus (CBUS). The CBUS carries control information that provides configuration and status exchanges between the source and the sink devices. CBUS is a software/hardware protocol that supports four types of packet transfers: Display Data Control (DDC), Vendor Specific, MHL Sideband Channel (MSC), and a reserved type. EDID data can be transferred

between the source and sink devices using the CBUS. On the SiI957n device, the CBUS signal pin is shared with the HPD signal pin. Another connection is used as the VBUS which provides +5V power to charge the connected MHL source device. An external power switch is typically used on the system board to supply the +5 V power to the VBUS. Enabling the switch provides the +5 V power on the VBUS when the MHL source is connected and the MHL cable detect signal is asserted.

6.7. 3D Video Formats on Main Display

The SiI957n port processor supports the pass-through of 3D video modes described in the HDMI 1.4a Specification. All modes support RGB 4:4:4, YCbCr 4:4:4, and YCbCr 4:2:2 color formats and 8-, 10-, and 12-bit data-width per color component. Table 6.3 shows only the maximum possible resolution with a given frame rate; for example, Side-by-Side (Half) mode is defined for 1080p @ 60 Hz, which implies that 720p, 60 Hz and 480p @ 60 Hz are also supported. Furthermore, a frame rate of 24 Hz also means that a frame rate of 23.98 Hz is supported and a frame rate of 60 Hz also means a frame rate of 59.94 Hz is supported. The input pixel clock changes accordingly.

The SiI957n device supports pass-through of the HDMI Vendor Specific InfoFrame, which carries 3D information to the receiver. It also supports extraction of the HDMI Vendor Specific InfoFrame, which allows the 3D information contained in the InfoFrame to be passed to the host system over the I^2C port.

Table 6.3. Supported 3D Video Formats

3D Format	Extended Definition	Resolution	Frame Rate (Hz)	Input Pixel Clock (MHz)
Frame Packing	—	1080p	50/60	297
Side-by-Side	Full			
Line Alternative	—			
L + Depth	—			
Frame Packing	—	1080p	24/30	148.5
		720p/1080i	50/60	
Side-by-Side	Full	1080p	24/30	
		720p/1080i	50/60	
	Half	1080p	50/60	
Top & Bottom	—	1080p	50/60	
		1080p	24/30	74.25
		720p/1080i	50/60	
Line Alternative	—	1080p	24/30	148.5
		720p/1080i	50/60	
Field Alternative	—	1080i	50/60	
L + Depth	—	1080p	24/30	

6.8. VS Insertion

The SiI957n device features logic that can be used to assist the downstream SoC in processing 3D video for display. It can monitor the 3D video stream and insert a VS pulse in the VS signal during the Active space period for demarcating the L and R video frames. Figure 6.2 on the next page shows the VS insertion mode. The front porch, pulse width, back porch, and polarity of the inserted VS signal can be individually set.

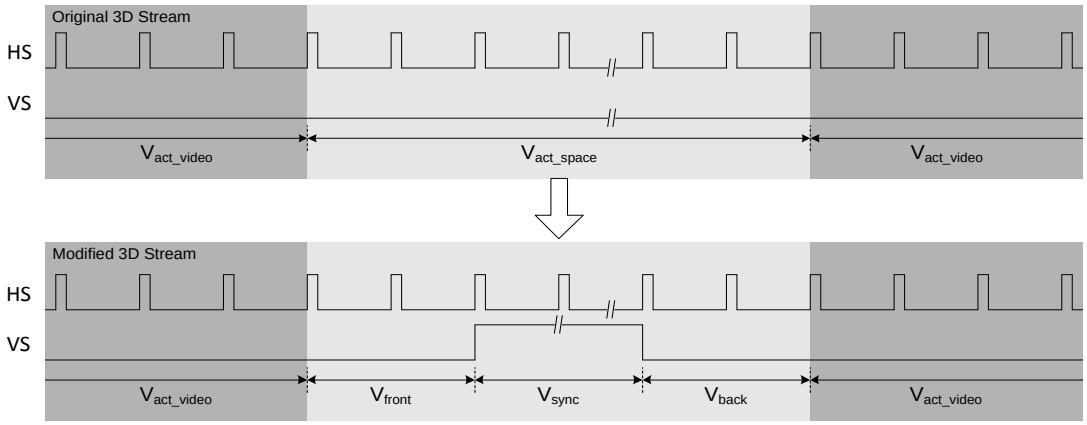


Figure 6.2. VS Insertion in Active Space

6.9. 3D L/R and Active Space Indicators Output on GPIO Pins

The SiI957n device can also monitor the 3D video stream and output L, R and Active Space indicators on GPIO pins for both the main pipe and the subpipe. The main pipe GPIO pins are shared with the main pipe I^2S audio extraction pins and the subpipe GPIO pins are shared with the SPI interface pins as shown in Table 6.4.

Table 6.4. L/R and Active Space Indicator Mapping to GPIO Pins

Pin	Name	Primary Function	Secondary Function
118	SCLK/GPIO3	SPI SCLK	SP_3D_R_FLAG
119	SDO/GPIO4	SPI SDO	SP_3D_V_FLAG
120	SDI/GPIO5	SPI SDI	SP_3D_L_FLAG
126	SD0_1/DR1/GPIO6	Audio Out I^2S/DSD	MP_3D_R_FLAG
127	SD0_2/DL1/GPIO7	Audio Out I^2S/DSD	MP_3D_V_FLAG
128	SD0_3/DR2/GPIO8	Audio Out I^2S/DSD	MP_3D_L_FLAG

The main pipe I^2S audio extraction must be disabled when the main pipe 3D indicators are output on the respective GPIO pins. The SPI interface to the external Flash memory cannot be used when the subpipe 3D indicators are output on the respective GPIO pins. Figure 6.3 shows the 3D L, R and Active Space indicators output on the respective GPIO pins. 3D indicators are supported only for 720p frame-packed, and 1080p frame-packed video modes.

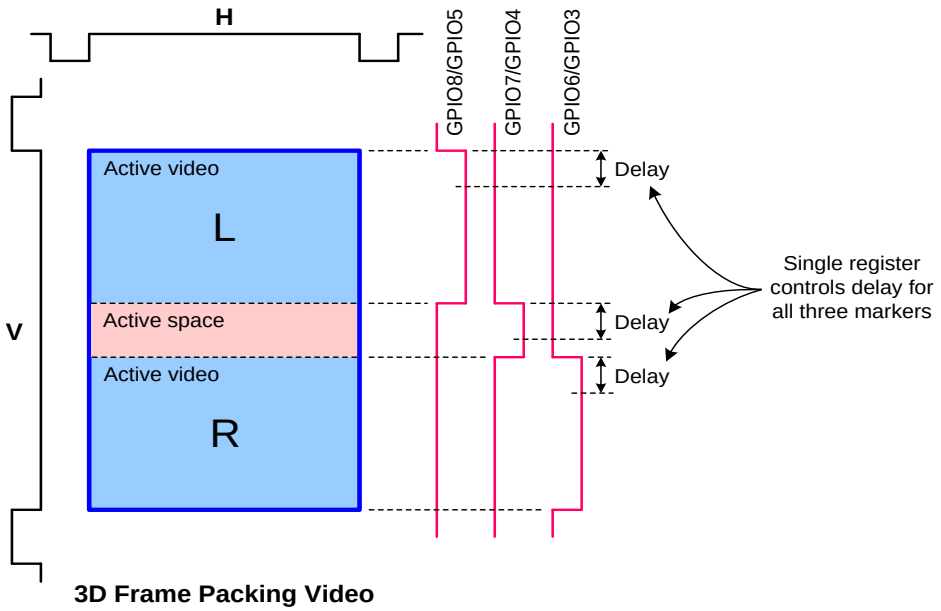


Figure 6.3. L/R and Active Space Indicators Output on GPIO Pins

6.10.Parallel Video Input Data Bus Mapping

6.10.1. Common Video Input Formats

Table 6.5. Video Input Formats

Color Space	Video Format	Clock Mode	Bus Width/ Color Depth	SYNC[4]	Input Clock (MHz)										Notes	Page
					480i[5]	VGA/ 480p	576i	576p	XGA	720p	1080i	SXGA	1080p	UXGA		
RGB	4:4:4	1x, dual	12/8	Sep	27	25/27	27	27	65	74.25	74.25	—	—	—	1	46
YCbCr	4:4:4	1x, dual	12/8	Sep	27	25/27	27	27	65	74.25	74.25	—	—	—	1	46
	4:2:2	1x, single	16/8 20/10	Sep	27	25/27	27	27	65	74.25	74.25	108	148.5	162	2	48
				Emb	27	25/27	27	27	65	74.25	74.25	108	148.5	162	2, 3	49
		2x, single/ YC Mux	8/8 10/10 12/12	Sep	—	50/54	54	54	130	148.5	148.5	—	—	—	2	52
				Emb	—	50/54	54	54	130	148.5	148.5	—	—	—	2, 3	56
		1x, dual/ YC Mux	8/8 10/10 12/12	Sep	27	25/27	27	27	65	74.25	74.25	108	148.5	162	1	—
				Emb	27	25/27	27	27	65	74.25	74.25	108	148.5	162	1, 3	—

Notes:

1. Falling or rising edge latched first is programmable.
2. Latching on falling or rising edge is programmable.
3. If embedded syncs are provided, DE is generated internally from SAV/EAV sequences. Embedded syncs use ITU-R BT 656 SAV/EAV sequences of FF, 00, 00, XY.
4. Sep = separate sync; Emb = embedded sync.
5. 480i must be provided at 27 MHz, using pixel replication, to be transmitted across the HDMI link.

6.10.2. RGB and YCbCr 4:4:4 Formats Dual Clock Edge

The input clock runs at the pixel rate and a complete definition of each pixel is received on each input clock cycle. One clock edge latches in half the pixel data. The opposite clock edge latches in the remaining half of the pixel data on the same pins. The same timing format is used for RGB and YCbCr 4:4:4. Each pair of columns in Table 6.6 shows the first pixel of *n + 1* pixels in the line of video. The figures below the table show RGB and YCbCr data; the YCbCr 4:4:4 data is given in braces {}. Data and control signals (D*x*, DE, HSYNC, and VSYNC) must change state to meet the setup and hold times specified for the dual edge mode, with respect to the *first* edge of IDCK as defined by the setting of the Edge Select bit (see the Programmer's Reference). The figures show IDCK latching input data when the Edge Select bit is set to *1* (first edge is the rising edge).

Table 6.6. RGB/YCbCr 4:4:4 Separate Sync Dual Clock Edge Data Mapping

Video Bus Setting	12-bit Data Bus 8-bit Color Depth		12-bit Data Bus 8-bit Color Depth		12-bit Data Bus 8-bit Color Depth		12-bit Data Bus 8-bit Color Depth	
YCSWAP	N/A		N/A		N/A		N/A	
DRA	0		1		0		1	
Pin Name	RGB		RGB		YCbCr		YCbCr	
	1st Clock Edge	2nd Clock Edge	1st Clock Edge	2nd Clock Edge	1st Clock Edge	2nd Clock Edge	1st Clock Edge	2nd Clock Edge
D0	LOW	LOW	B0[0]	G0[4]	LOW	LOW	Cb0[0]	Y0[4]
D1	LOW	LOW	B0[1]	G0[5]	LOW	LOW	Cb0[1]	Y0[5]
D2	LOW	LOW	B0[2]	G0[6]	LOW	LOW	Cb0[2]	Y0[6]
D3	LOW	LOW	B0[3]	G0[7]	LOW	LOW	Cb0[3]	Y0[7]
D4	LOW	LOW	B0[4]	R0[0]	LOW	LOW	Cb0[4]	Cr0[0]
D5	LOW	LOW	B0[5]	R0[1]	LOW	LOW	Cb0[5]	Cr0[1]
D6	LOW	LOW	B0[6]	R0[2]	LOW	LOW	Cb0[6]	Cr0[2]
D7	LOW	LOW	B0[7]	R0[3]	LOW	LOW	Cb0[7]	Cr0[3]
D8	B0[0]	G0[4]	G0[0]	R0[4]	Cb0[0]	Y0[4]	Y0[0]	Cr0[4]
D9	B0[1]	G0[5]	G0[1]	R0[5]	Cb0[1]	Y0[5]	Y0[1]	Cr0[5]
D10	B0[2]	G0[6]	G0[2]	R0[6]	Cb0[2]	Y0[6]	Y0[2]	Cr0[6]
D11	B0[3]	G0[7]	G0[3]	R0[7]	Cb0[3]	Y0[7]	Y0[3]	Cr0[7]
D12	B0[4]	R0[0]	LOW	LOW	Cb0[4]	Cr0[0]	LOW	LOW
D13	B0[5]	R0[1]	LOW	LOW	Cb0[5]	Cr0[1]	LOW	LOW
D14	B0[6]	R0[2]	LOW	LOW	Cb0[6]	Cr0[2]	LOW	LOW
D15	B0[7]	R0[3]	LOW	LOW	Cb0[7]	Cr0[3]	LOW	LOW
D16	G0[0]	R0[4]	LOW	LOW	Y0[0]	Cr0[4]	LOW	LOW
D17	G0[1]	R0[5]	LOW	LOW	Y0[1]	Cr0[5]	LOW	LOW
D18	G0[2]	R0[6]	LOW	LOW	Y0[2]	Cr0[6]	LOW	LOW
D19	G0[3]	R0[7]	LOW	LOW	Y0[3]	Cr0[7]	LOW	LOW
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE	DE	DE

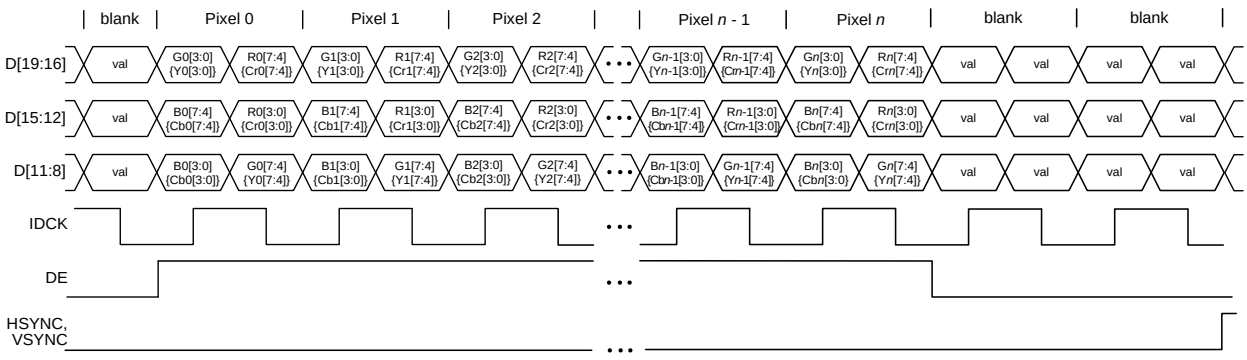


Figure 6.4. 8-bit Color Depth RGB/YCbCr 4:4:4 Dual Edge Timing (DRA = 0)

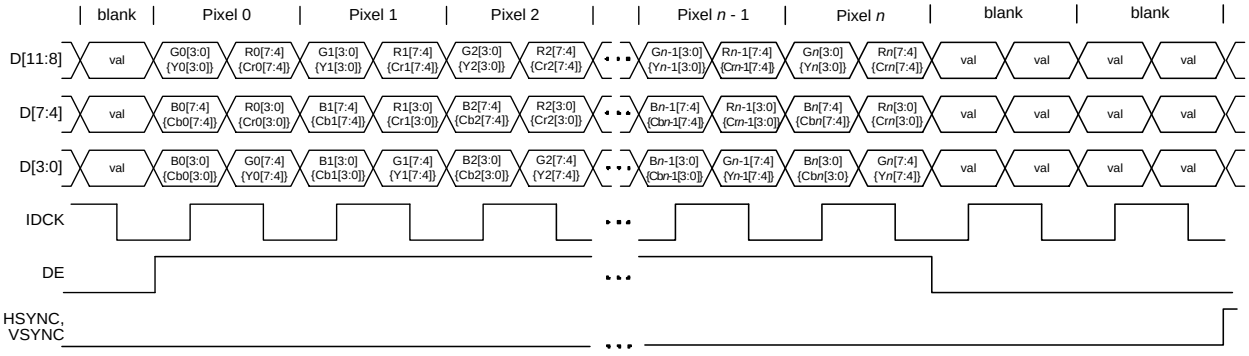


Figure 6.5. 8-bit Color Depth RGB/YCbCr 4:4:4 Dual Edge Timing (DRA = 1)

6.10.3. YC 4:2:2 Separate Sync Formats

The input clock runs at the pixel rate and a complete definition of each pixel is received on each input clock cycle. A luma (Y) value is carried for every pixel, but the chroma values (Cb and Cr) change only every second pixel. The data bus can be 16 or 20 bits. HSYNC and VSYNC are driven explicitly on their own signals. Each pair of columns in Table 6.7 shows the first and second pixel of *n + 1* pixels in the line of video. The DE HIGH time must contain an even number of pixel clocks.

Table 6.7. YC 4:2:2 Separate Sync Data Mapping

Video Bus Setting	16-bit Data Bus 8-bit Color Depth		16-bit Data Bus 8-bit Color Depth		20-bit Data Bus 10-bit Color Depth		20-bit Data Bus 10-bit Color Depth	
YCSWAP	0		1		0		1	
DRA	N/A		N/A		N/A		N/A	
Pin Name	**Pixel #0**	**Pixel #1**	**Pixel #0**	**Pixel #1**	**Pixel #0**	**Pixel #1**	**Pixel #0**	**Pixel #1**
D0	LOW	LOW	LOW	LOW	Cb0[0]	Cr0[0]	Y0[0]	Y1[0]
D1	LOW	LOW	LOW	LOW	Cb0[1]	Cr0[1]	Y0[1]	Y1[1]
D2	Cb0[0]	Cr0[0]	Y0[0]	Y1[0]	Cb0[2]	Cr0[2]	Y0[2]	Y1[2]
D3	Cb0[1]	Cr0[1]	Y0[1]	Y1[1]	Cb0[3]	Cr0[3]	Y0[3]	Y1[3]
D4	Cb0[2]	Cr0[2]	Y0[2]	Y1[2]	Cb0[4]	Cr0[4]	Y0[4]	Y1[4]
D5	Cb0[3]	Cr0[3]	Y0[3]	Y1[3]	Cb0[5]	Cr0[5]	Y0[5]	Y1[5]
D6	Cb0[4]	Cr0[4]	Y0[4]	Y1[4]	Cb0[6]	Cr0[6]	Y0[6]	Y1[6]
D7	Cb0[5]	Cr0[5]	Y0[5]	Y1[5]	Cb0[7]	Cr0[7]	Y0[7]	Y1[7]
D8	Cb0[6]	Cr0[6]	Y0[6]	Y1[6]	Cb0[8]	Cr0[8]	Y0[8]	Y1[8]
D9	Cb0[7]	Cr0[7]	Y0[7]	Y1[7]	Cb0[9]	Cr0[9]	Y0[9]	Y1[9]
D10	LOW	LOW	LOW	LOW	Y0[0]	Y1[0]	Cb0[0]	Cr0[0]
D11	LOW	LOW	LOW	LOW	Y0[1]	Y1[1]	Cb0[1]	Cr0[1]
D12	Y0[0]	Y1[0]	Cb0[0]	Cr0[0]	Y0[2]	Y1[2]	Cb0[2]	Cr0[2]
D13	Y0[1]	Y1[1]	Cb0[1]	Cr0[1]	Y0[3]	Y1[3]	Cb0[3]	Cr0[3]
D14	Y0[2]	Y1[2]	Cb0[2]	Cr0[2]	Y0[4]	Y1[4]	Cb0[4]	Cr0[4]
D15	Y0[3]	Y1[3]	Cb0[3]	Cr0[3]	Y0[5]	Y1[5]	Cb0[5]	Cr0[5]
D16	Y0[4]	Y1[4]	Cb0[4]	Cr0[4]	Y0[6]	Y1[6]	Cb0[6]	Cr0[6]
D17	Y0[5]	Y1[5]	Cb0[5]	Cr0[5]	Y0[7]	Y1[7]	Cb0[7]	Cr0[7]
D18	Y0[6]	Y1[6]	Cb0[6]	Cr0[6]	Y0[8]	Y1[8]	Cb0[8]	Cr0[8]
D19	Y0[7]	Y1[7]	Cb0[7]	Cr0[7]	Y0[9]	Y1[9]	Cb0[9]	Cr0[9]
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE	DE	DE

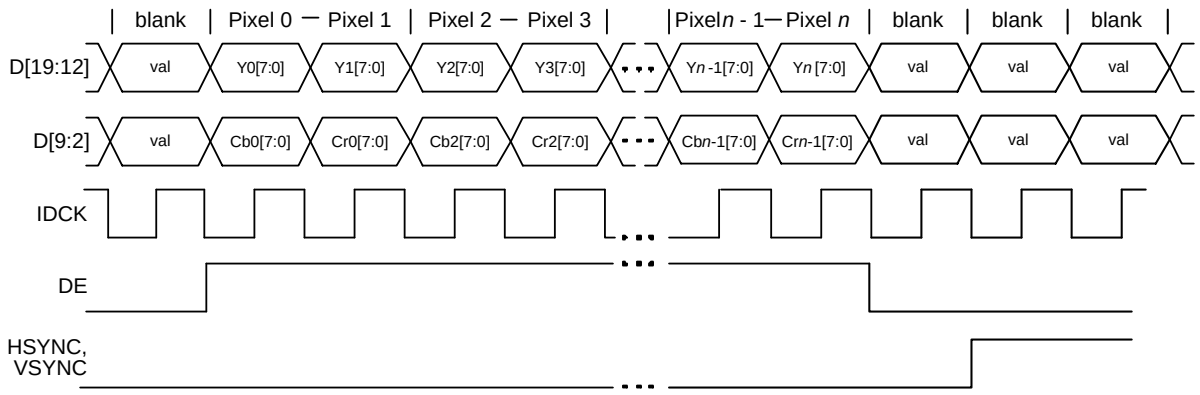


Figure 6.6. 8-bit Color Depth YC 4:2:2 Timing (YCSWAP = 0)

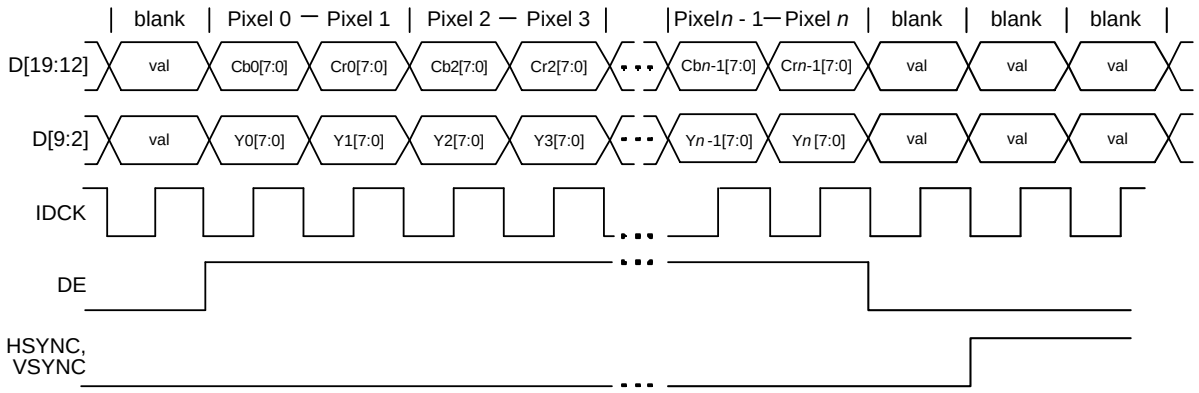


Figure 6.7. 8-bit Color Depth YC 4:2:2 Timing (YCSWAP = 1)

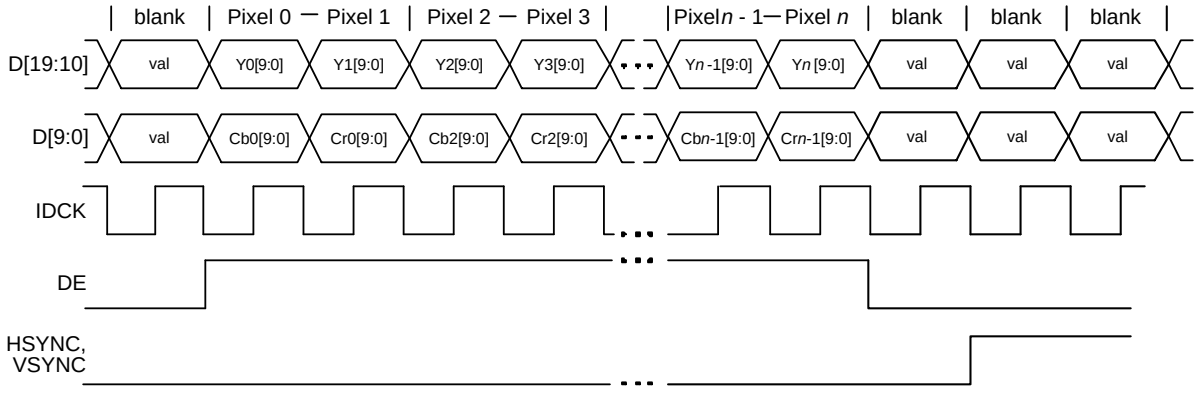


Figure 6.8. 10-bit Color Depth YC 4:2:2 Timing (YCSWAP = 0)

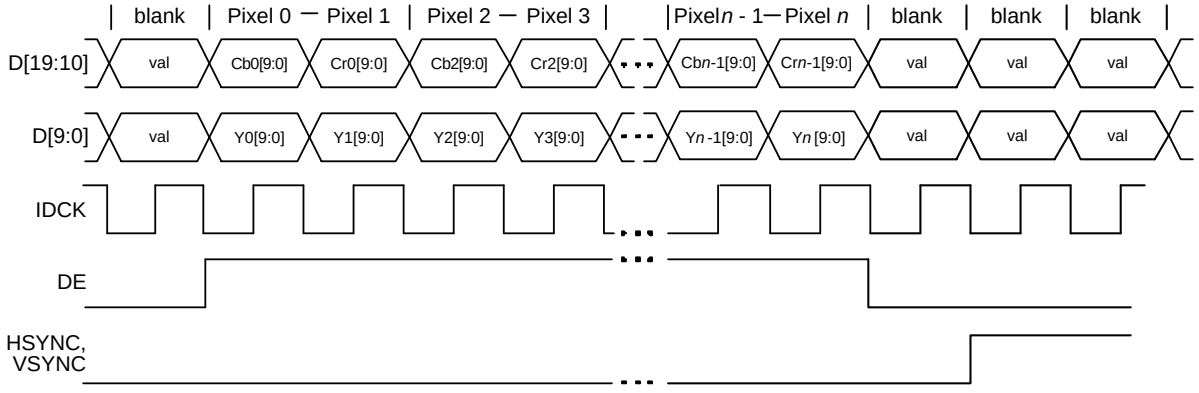


Figure 6.9. 10-bit Color Depth YC 4:2:2 Timing (YCSWAP = 1)

6.10.4. YC 4:2:2 Embedded Syncs Formats

The Embedded Sync format is identical to the YC 4:2:2 formats with Separate Syncs, except that the syncs are embedded and not explicit. The data bus is 16 bits. Each pair of columns in Table 6.8 shows the first and second pixel of *n + 1* pixels in the line of video.

Table 6.8. YC 4:2:2 Embedded Sync Data Mapping

Video Bus Setting	16-bit Data Bus 8-bit Color Depth		16-bit Data Bus 8-bit Color Depth		20-bit Data Bus 10-bit Color Depth		20-bit Data Bus 10-bit Color Depth	
YCSWAP	0		1		0		1	
DRA	N/A		N/A		N/A		N/A	
Pin Name	**Pixel #0**	**Pixel #1**	**Pixel #0**	**Pixel #1**	**Pixel #0**	**Pixel #1**	**Pixel #0**	**Pixel #1**
D0	LOW	LOW	LOW	LOW	Cb0[0]	Cr0[0]	Y0[0]	Y1[0]
D1	LOW	LOW	LOW	LOW	Cb0[1]	Cr0[1]	Y0[1]	Y1[1]
D2	Cb0[0]	Cr0[0]	Y0[0]	Y1[0]	Cb0[2]	Cr0[2]	Y0[2]	Y1[2]
D3	Cb0[1]	Cr0[1]	Y0[1]	Y1[1]	Cb0[3]	Cr0[3]	Y0[3]	Y1[3]
D4	Cb0[2]	Cr0[2]	Y0[2]	Y1[2]	Cb0[4]	Cr0[4]	Y0[4]	Y1[4]
D5	Cb0[3]	Cr0[3]	Y0[3]	Y1[3]	Cb0[5]	Cr0[5]	Y0[5]	Y1[5]
D6	Cb0[4]	Cr0[4]	Y0[4]	Y1[4]	Cb0[6]	Cr0[6]	Y0[6]	Y1[6]
D7	Cb0[5]	Cr0[5]	Y0[5]	Y1[5]	Cb0[7]	Cr0[7]	Y0[7]	Y1[7]
D8	Cb0[6]	Cr0[6]	Y0[6]	Y1[6]	Cb0[8]	Cr0[8]	Y0[8]	Y1[8]
D9	Cb0[7]	Cr0[7]	Y0[7]	Y1[7]	Cb0[9]	Cr0[9]	Y0[9]	Y1[9]
D10	LOW	LOW	LOW	LOW	Y0[0]	Y1[0]	Cb0[0]	Cr0[0]
D11	LOW	LOW	LOW	LOW	Y0[1]	Y1[1]	Cb0[1]	Cr0[1]
D12	Y0[0]	Y1[0]	Cb0[0]	Cr0[0]	Y0[2]	Y1[2]	Cb0[2]	Cr0[2]
D13	Y0[1]	Y1[1]	Cb0[1]	Cr0[1]	Y0[3]	Y1[3]	Cb0[3]	Cr0[3]
D14	Y0[2]	Y1[2]	Cb0[2]	Cr0[2]	Y0[4]	Y1[4]	Cb0[4]	Cr0[4]
D15	Y0[3]	Y1[3]	Cb0[3]	Cr0[3]	Y0[5]	Y1[5]	Cb0[5]	Cr0[5]
D16	Y0[4]	Y1[4]	Cb0[4]	Cr0[4]	Y0[6]	Y1[6]	Cb0[6]	Cr0[6]
D17	Y0[5]	Y1[5]	Cb0[5]	Cr0[5]	Y0[7]	Y1[7]	Cb0[7]	Cr0[7]
D18	Y0[6]	Y1[6]	Cb0[6]	Cr0[6]	Y0[8]	Y1[8]	Cb0[8]	Cr0[8]
D19	Y0[7]	Y1[7]	Cb0[7]	Cr0[7]	Y0[9]	Y1[9]	Cb0[9]	Cr0[9]
HSYNC	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
VSYNC	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
DE	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

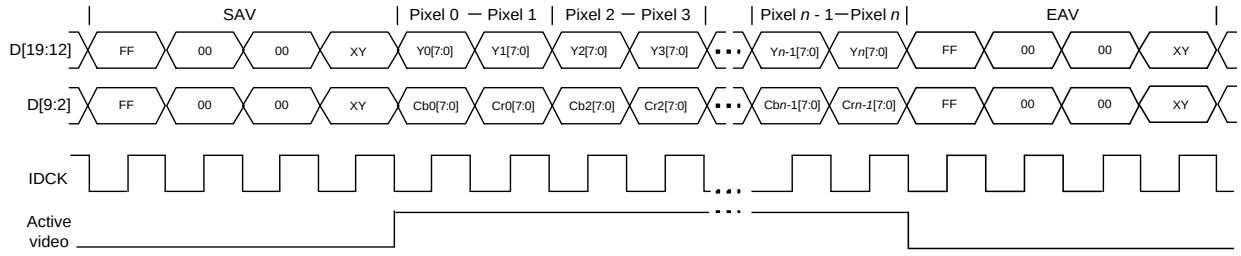


Figure 6.10. 8-bit Color Depth YC 4:2:2 Embedded Sync Timing (YCSWAP = 0)

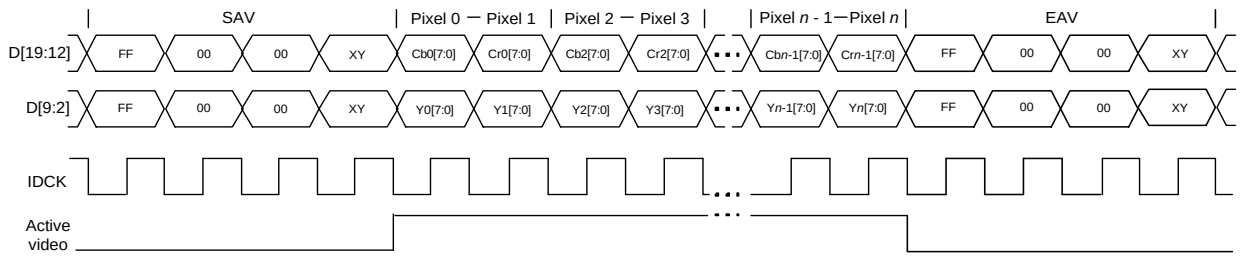


Figure 6.11. 8-bit Color Depth YC 4:2:2 Embedded Sync Timing (YCSWAP = 1)

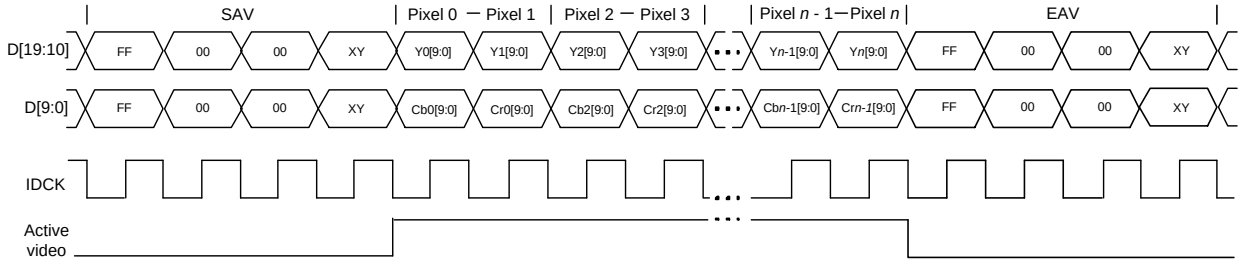


Figure 6.12. 10-bit Color Depth YC 4:2:2 Embedded Sync Timing (YCSWAP = 0)

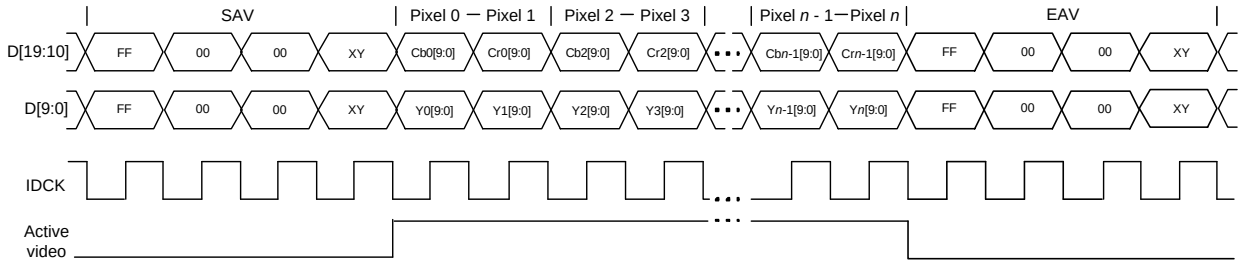


Figure 6.13. 10-bit Color Depth YC 4:2:2 Embedded Sync Timing (YCSWAP = 1)

6.10.5. YC Mux 4:2:2 Separate Sync Formats Single Clock Edge

The video data is multiplexed onto fewer pins than the mapping described in the YC 4:2:2 Separate Sync Formats section on page 48. The input clock runs at double the pixel rate so a chroma value is sent for each pixel, followed by a corresponding luma value for the same pixel. Thus, a luma (Y) value is provided for each pixel, while the Cb and Cr values alternate on successive pixels. Each group of four columns in Table 6.9 shows the four clock cycles for the first two pixels of the line. Pixel values for Cb0 and Y0 values are sent with the first pixel (first two clock cycles). Then the Cr0 and Y1 values are sent with the second pixel (next two clock cycles). The figures below the table show how this pattern is extended for the rest of the pixels in a video line of *n + 1* pixels.

Table 6.9. YC Mux 4:2:2 8-bit Color Depth Separate Sync Data Mapping

Video Bus Setting	8-bit Data Bus 8-bit Color Depth				8-bit Data Bus 8-bit Color Depth			
YCSWAP	N/A				N/A			
DRA	0				1			
Pin Name	Pixel #0		Pixel #1		Pixel #0		Pixel #1	
	1st Clock Cycle	2nd Clock Cycle	3rd Clock Cycle	4th Clock Cycle	1st Clock Cycle	2nd Clock Cycle	3rd Clock Cycle	4th Clock Cycle
D0	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
D1	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
D2	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
D3	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
D4	LOW	LOW	LOW	LOW	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]
D5	LOW	LOW	LOW	LOW	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]
D6	LOW	LOW	LOW	LOW	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]
D7	LOW	LOW	LOW	LOW	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]
D8	LOW	LOW	LOW	LOW	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]
D9	LOW	LOW	LOW	LOW	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]
D10	LOW	LOW	LOW	LOW	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]
D11	LOW	LOW	LOW	LOW	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]
D12	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	LOW	LOW	LOW	LOW
D13	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	LOW	LOW	LOW	LOW
D14	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	LOW	LOW	LOW	LOW
D15	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	LOW	LOW	LOW	LOW
D16	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	LOW	LOW	LOW	LOW
D17	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	LOW	LOW	LOW	LOW
D18	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	LOW	LOW	LOW	LOW
D19	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	LOW	LOW	LOW	LOW
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE	DE	DE

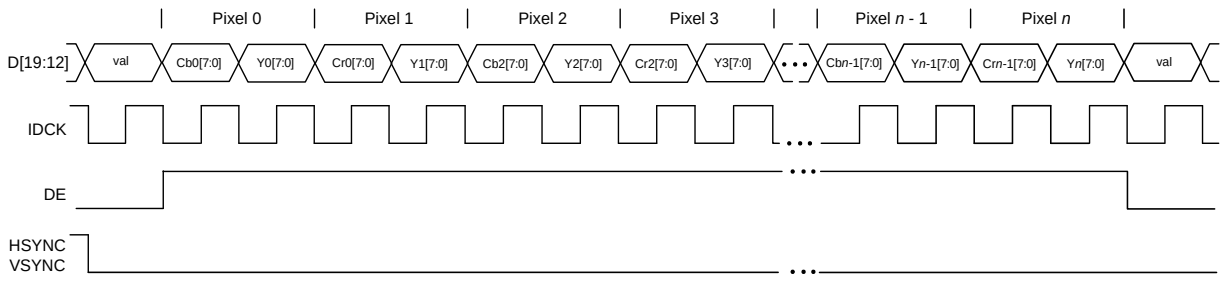


Figure 6.14. 8-bit Color Depth YC Mux 4:2:2 Timing (DRA = 0)

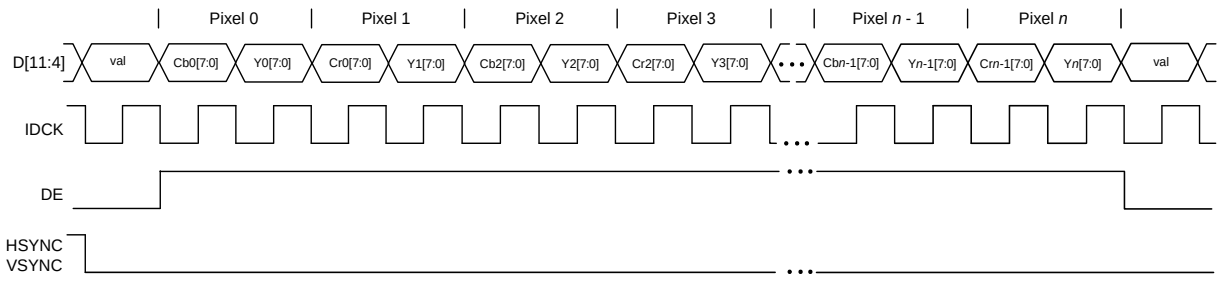


Figure 6.15. 8-bit Color Depth YC Mux 4:2:2 Timing (DRA = 1)

Table 6.10. YC Mux 4:2:2 10-bit Color Depth Separate Sync Data Mapping

Video Bus Setting	10-bit Data Bus 10-bit Color Depth				10-bit Data Bus 10-bit Color Depth			
YCSWAP	N/A				N/A			
DRA	0				1			
Pin Name	Pixel #0		Pixel #1		Pixel #0		Pixel #1	
	1st Clock Cycle	2nd Clock Cycle	3rd Clock Cycle	4th Clock Cycle	1st Clock Cycle	2nd Clock Cycle	3rd Clock Cycle	4th Clock Cycle
D0	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
D1	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
D2	LOW	LOW	LOW	LOW	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]
D3	LOW	LOW	LOW	LOW	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]
D4	LOW	LOW	LOW	LOW	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]
D5	LOW	LOW	LOW	LOW	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]
D6	LOW	LOW	LOW	LOW	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]
D7	LOW	LOW	LOW	LOW	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]
D8	LOW	LOW	LOW	LOW	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]
D9	LOW	LOW	LOW	LOW	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]
D10	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]
D11	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]
D12	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	LOW	LOW	LOW	LOW
D13	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	LOW	LOW	LOW	LOW
D14	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	LOW	LOW	LOW	LOW
D15	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	LOW	LOW	LOW	LOW
D16	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	LOW	LOW	LOW	LOW
D17	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	LOW	LOW	LOW	LOW
D18	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]	LOW	LOW	LOW	LOW
D19	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]	LOW	LOW	LOW	LOW
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE	DE	DE

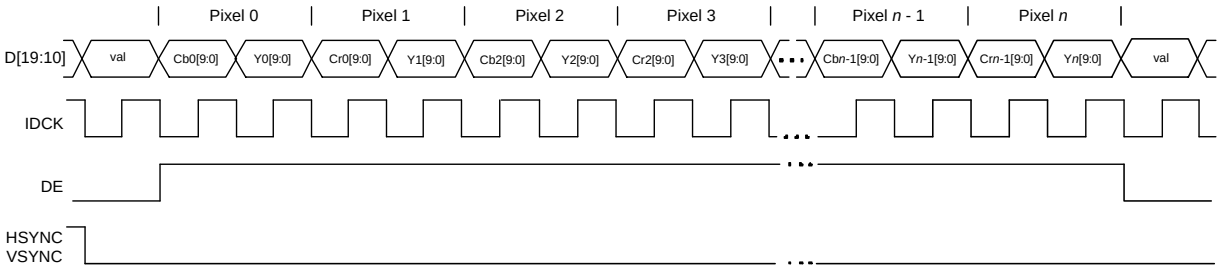


Figure 6.16. 10-bit Color Depth YC Mux 4:2:2 Timing (DRA = 0)

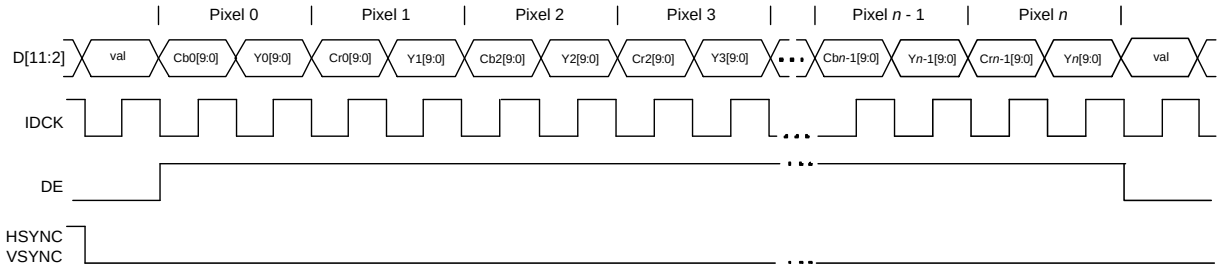


Figure 6.17. 10-bit Color Depth YC Mux 4:2:2 Timing (DRA = 1)

Table 6.11. YC Mux 4:2:2 12-bit Color Depth Separate Sync Data Mapping

Video Bus Setting	12-bit Data Bus 12-bit Color Depth				12-bit Data Bus 12-bit Color Depth			
YCSWAP	N/A				N/A			
DRA	0				1			
Pin Name	Pixel #0		Pixel #1		Pixel #0		Pixel #1	
	1st Clock Cycle	2nd Clock Cycle	3rd Clock Cycle	4th Clock Cycle	1st Clock Cycle	2nd Clock Cycle	3rd Clock Cycle	4th Clock Cycle
D0	LOW	LOW	LOW	LOW	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]
D1	LOW	LOW	LOW	LOW	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]
D2	LOW	LOW	LOW	LOW	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]
D3	LOW	LOW	LOW	LOW	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]
D4	LOW	LOW	LOW	LOW	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]
D5	LOW	LOW	LOW	LOW	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]
D6	LOW	LOW	LOW	LOW	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]
D7	LOW	LOW	LOW	LOW	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]
D8	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]
D9	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]
D10	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	Cb0[10]	Y0[10]	Cr0[10]	Y1[10]
D11	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	Cb0[11]	Y0[11]	Cr0[11]	Y1[11]
D12	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	LOW	LOW	LOW	LOW
D13	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	LOW	LOW	LOW	LOW
D14	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	LOW	LOW	LOW	LOW
D15	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	LOW	LOW	LOW	LOW
D16	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]	LOW	LOW	LOW	LOW
D17	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]	LOW	LOW	LOW	LOW
D18	Cb0[10]	Y0[10]	Cr0[10]	Y1[10]	LOW	LOW	LOW	LOW
D19	Cb0[11]	Y0[11]	Cr0[11]	Y1[11]	LOW	LOW	LOW	LOW
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE	DE	DE

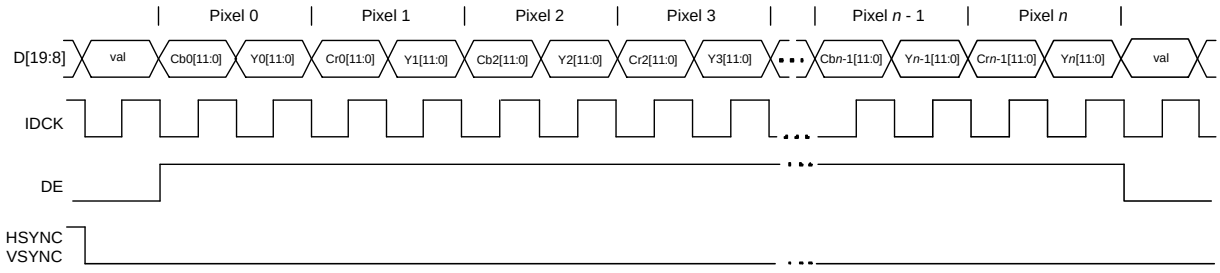


Figure 6.18. 12-bit Color Depth YC Mux 4:2:2 Timing (DRA = 0)

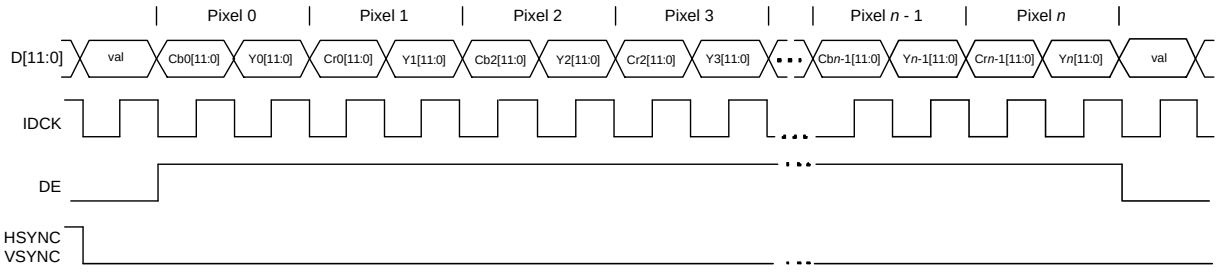


Figure 6.19. 12-bit Color Depth YC Mux 4:2:2 Timing (DRA = 1)

6.10.6. YC Mux 4:2:2 Embedded Sync Formats Single Clock Edge

This format is identical to the one described in the YC Mux 4:2:2 Separate Sync Formats Single Clock Edge section on page 52, except the syncs are embedded and not explicit. The figures following this table show only the first two pixels and last pixel of the line and the SAV and EAV sequences, but the remaining pixels are similar to those shown in the figures of the previous section.

Table 6.12. YC Mux 4:2:2 8-bit Color Depth Embedded Sync Data Mapping

Video Bus Setting	8-bit Data Bus 8-bit Color Depth				8-bit Data Bus 8-bit Color Depth			
YCSWAP	N/A				N/A			
DRA	0				1			
Pin Name	Pixel #0		Pixel #1		Pixel #0		Pixel #1	
	1st Clock Cycle	2nd Clock Cycle	3rd Clock Cycle	4th Clock Cycle	1st Clock Cycle	2nd Clock Cycle	3rd Clock Cycle	4th Clock Cycle
D0	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
D1	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
D2	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
D3	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
D4	LOW	LOW	LOW	LOW	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]
D5	LOW	LOW	LOW	LOW	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]
D6	LOW	LOW	LOW	LOW	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]
D7	LOW	LOW	LOW	LOW	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]
D8	LOW	LOW	LOW	LOW	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]
D9	LOW	LOW	LOW	LOW	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]
D10	LOW	LOW	LOW	LOW	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]
D11	LOW	LOW	LOW	LOW	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]
D12	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	LOW	LOW	LOW	LOW
D13	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	LOW	LOW	LOW	LOW
D14	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	LOW	LOW	LOW	LOW
D15	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	LOW	LOW	LOW	LOW
D16	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	LOW	LOW	LOW	LOW
D17	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	LOW	LOW	LOW	LOW
D18	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	LOW	LOW	LOW	LOW
D19	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	LOW	LOW	LOW	LOW
HSYNC	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
VSYNC	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
DE	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

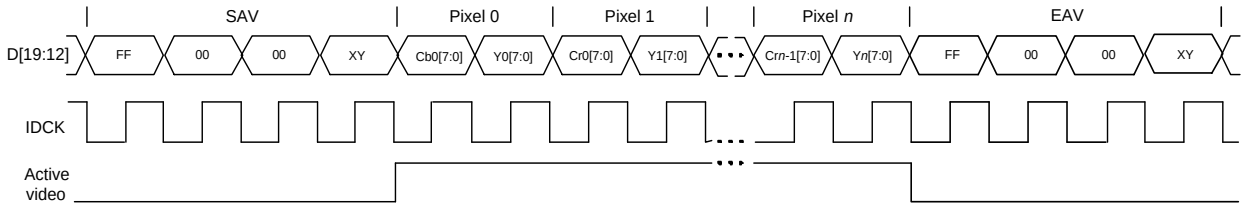


Figure 6.20. 8-bit Color Depth YC Mux 4:2:2 Embedded Sync Timing (DRA = 0)

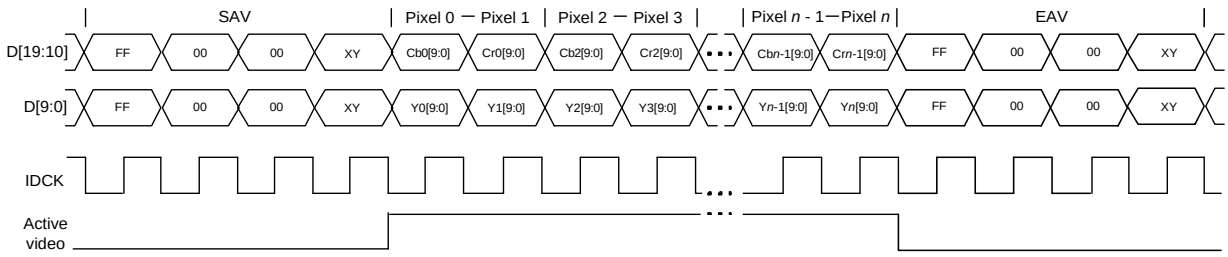


Figure 6.21. 8-bit Color Depth YC Mux 4:2:2 Embedded Sync Timing (DRA = 1)

Table 6.13. YC Mux 4:2:2 10-bit Color Depth Embedded Sync Data Mapping

Video Bus Setting	10-bit Data Bus 10-bit Color Depth				10-bit Data Bus 10-bit Color Depth			
YCSWAP	N/A				N/A			
DRA	0				1			
Pin Name	Pixel #0		Pixel #1		Pixel #0		Pixel #1	
	1st Clock Cycle	2nd Clock Cycle	3rd Clock Cycle	4th Clock Cycle	1st Clock Cycle	2nd Clock Cycle	3rd Clock Cycle	4th Clock Cycle
D0	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
D1	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
D2	LOW	LOW	LOW	LOW	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]
D3	LOW	LOW	LOW	LOW	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]
D4	LOW	LOW	LOW	LOW	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]
D5	LOW	LOW	LOW	LOW	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]
D6	LOW	LOW	LOW	LOW	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]
D7	LOW	LOW	LOW	LOW	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]
D8	LOW	LOW	LOW	LOW	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]
D9	LOW	LOW	LOW	LOW	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]
D10	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]
D11	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]
D12	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	LOW	LOW	LOW	LOW
D13	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	LOW	LOW	LOW	LOW
D14	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	LOW	LOW	LOW	LOW
D15	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	LOW	LOW	LOW	LOW
D16	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	LOW	LOW	LOW	LOW
D17	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	LOW	LOW	LOW	LOW
D18	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]	LOW	LOW	LOW	LOW
D19	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]	LOW	LOW	LOW	LOW
HSYNC	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
VSYNC	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
DE	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

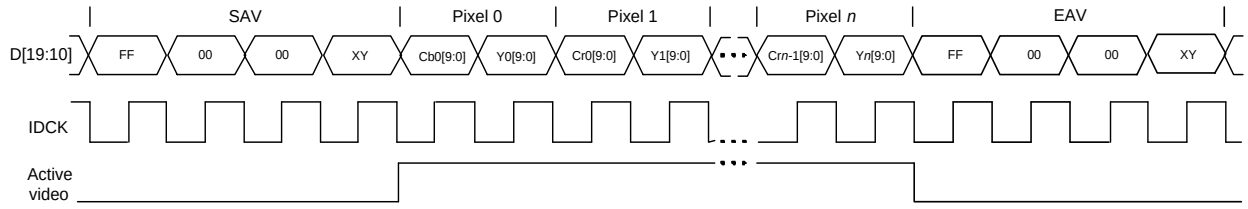


Figure 6.22. 10-bit Color Depth YC Mux 4:2:2 Embedded Sync Timing (DRA = 0)

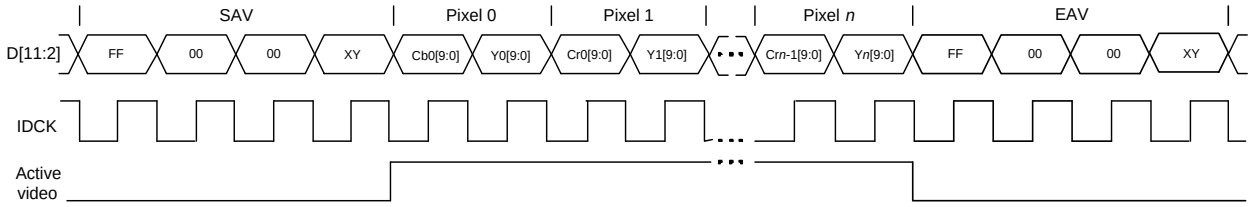


Figure 6.23. 10-bit Color Depth YC Mux 4:2:2 Embedded Sync Timing (DRA = 1)

Table 6.14. YC Mux 4:2:2 12-bit Color Depth Embedded Sync Data Mapping

Video Bus Setting	12-bit Data Bus 12-bit Color Depth				12-bit Data Bus 12-bit Color Depth			
YCSWAP	N/A				N/A			
DRA	0				1			
Pin Name	Pixel #0		Pixel #1		Pixel #0		Pixel #1	
	1st Clock Cycle	2nd Clock Cycle	3rd Clock Cycle	4th Clock Cycle	1st Clock Cycle	2nd Clock Cycle	3rd Clock Cycle	4th Clock Cycle
D0	LOW	LOW	LOW	LOW	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]
D1	LOW	LOW	LOW	LOW	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]
D2	LOW	LOW	LOW	LOW	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]
D3	LOW	LOW	LOW	LOW	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]
D4	LOW	LOW	LOW	LOW	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]
D5	LOW	LOW	LOW	LOW	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]
D6	LOW	LOW	LOW	LOW	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]
D7	LOW	LOW	LOW	LOW	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]
D8	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]
D9	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]
D10	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	Cb0[10]	Y0[10]	Cr0[10]	Y1[10]
D11	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	Cb0[11]	Y0[11]	Cr0[11]	Y1[11]
D12	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	LOW	LOW	LOW	LOW
D13	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	LOW	LOW	LOW	LOW
D14	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	LOW	LOW	LOW	LOW
D15	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	LOW	LOW	LOW	LOW
D16	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]	LOW	LOW	LOW	LOW
D17	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]	LOW	LOW	LOW	LOW
D18	Cb0[10]	Y0[10]	Cr0[10]	Y1[10]	LOW	LOW	LOW	LOW
D19	Cb0[11]	Y0[11]	Cr0[11]	Y1[11]	LOW	LOW	LOW	LOW
HSYNC	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
VSYNC	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
DE	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

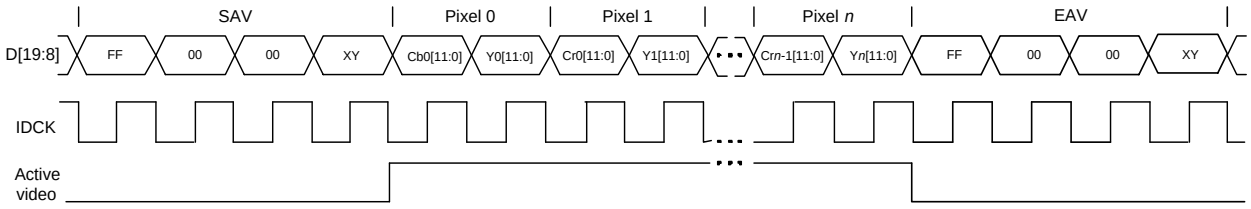


Figure 6.24. 12-bit Color Depth YC Mux 4:2:2 Embedded Sync Timing (DRA = 0)

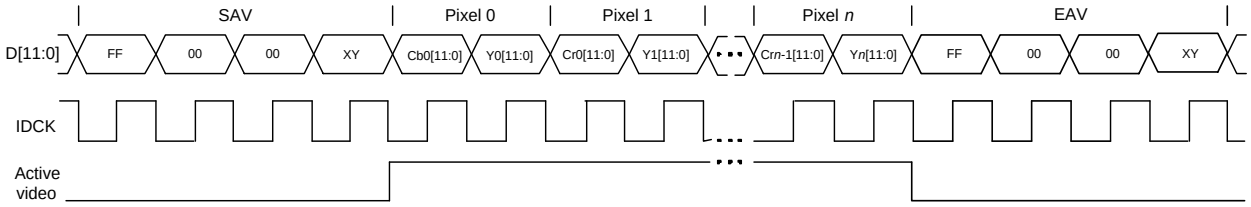


Figure 6.25. 12-bit Color Depth YC Mux 4:2:2 Embedded Sync Timing (DRA = 1)

6.10.7. YC Mux 4:2:2 Separate Sync Formats Dual Clock Edge

The video data is multiplexed onto fewer pins than the mapping described in the YC 4:2:2 Separate Sync Formats on page 48. The input clock runs at the pixel rate and a complete definition of each pixel is received on each input clock cycle. The chroma value is sent for each pixel, followed by a corresponding luma value for the same pixel. Thus, a luma (Y) value is provided for each pixel, while the Cb and Cr values alternate on successive pixels. One clock edge latches in half the pixel data. The opposite clock edge latches in the remaining half of the pixel data on the same pins.

Each group of four columns in Table 6.9 shows the two clock cycles for the first two pixels of the line. Pixel values for Cb0 and Y0 values are sent with the first pixel (first and second clock edges of the first clock cycle). Then the Cr0 and Y1 values are sent with the second pixel (first and second clock edges of the second clock cycle). The figures below the table show how this pattern is extended for the rest of the pixels in a video line of *n + 1* pixels.

Table 6.15. YC Mux 4:2:2 8-bit Color Depth Separate Sync Dual Clock Edge Data Mapping

Video Bus Setting	8-bit Data Bus 8-bit Color Depth				8-bit Data Bus 8-bit Color Depth			
YCSWAP	0				1			
DRA	0				1			
Pin Name	Pixel #0		Pixel #1		Pixel #0		Pixel #1	
	1st Clock		2nd Clock		1st Clock		2nd Clock	
	1st Clock Edge	2nd Clock Edge	1st Clock Edge	2nd Clock Edge	1st Clock Edge	2nd Clock Edge	1st Clock Edge	2nd Clock Edge
D0	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
D1	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
D2	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
D3	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
D4	LOW	LOW	LOW	LOW	Y0[0]	Cb0[0]	Y1[0]	Cr0[0]
D5	LOW	LOW	LOW	LOW	Y0[1]	Cb0[1]	Y1[1]	Cr0[1]
D6	LOW	LOW	LOW	LOW	Y0[2]	Cb0[2]	Y1[2]	Cr0[2]
D7	LOW	LOW	LOW	LOW	Y0[3]	Cb0[3]	Y1[3]	Cr0[3]
D8	LOW	LOW	LOW	LOW	Y0[4]	Cb0[4]	Y1[4]	Cr0[4]
D9	LOW	LOW	LOW	LOW	Y0[5]	Cb0[5]	Y1[5]	Cr0[5]
D10	LOW	LOW	LOW	LOW	Y0[6]	Cb0[6]	Y1[6]	Cr0[6]
D11	LOW	LOW	LOW	LOW	Y0[7]	Cb0[7]	Y1[7]	Cr0[7]
D12	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	LOW	LOW	LOW	LOW
D13	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	LOW	LOW	LOW	LOW
D14	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	LOW	LOW	LOW	LOW
D15	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	LOW	LOW	LOW	LOW
D16	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	LOW	LOW	LOW	LOW
D17	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	LOW	LOW	LOW	LOW
D18	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	LOW	LOW	LOW	LOW
D19	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	LOW	LOW	LOW	LOW
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE	DE	DE

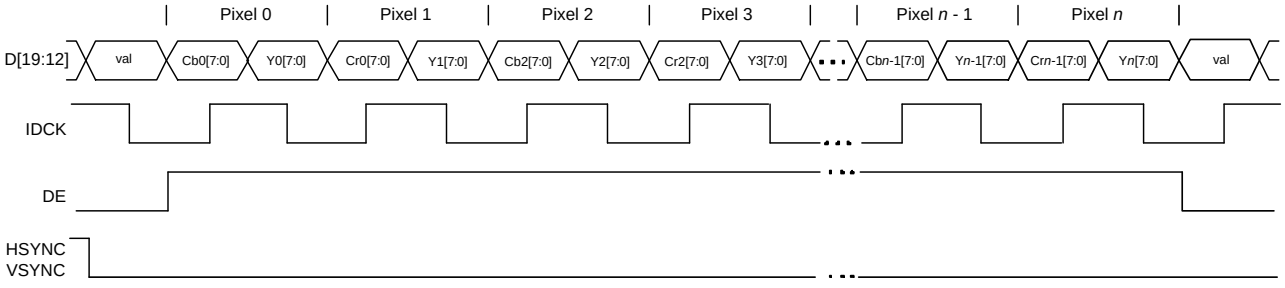


Figure 6.26. 8-bit Color Depth YC Mux 4:2:2 Dual Edge Timing (DRA = 0, YCSWAP = 0)

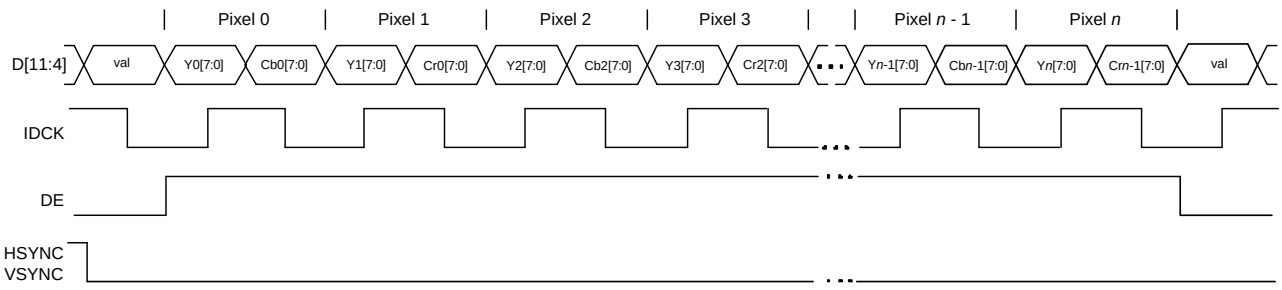


Figure 6.27. 8-bit Color Depth YC Mux 4:2:2 Dual Edge Timing (DRA = 1, YCSWAP = 1)

Table 6.16. YC Mux 4:2:2 10-bit Color Depth Separate Sync Dual Clock Edge Data Mapping

Video Bus Setting	10-bit Data Bus 10-bit Color Depth				10-bit Data Bus 10-bit Color Depth			
YCSWAP	0				0			
DRA	0				1			
Pin Name	Pixel #0		Pixel #1		Pixel #0		Pixel #1	
	1st Clock		2nd Clock		1st Clock		2nd Clock	
	1st Clock Edge	2nd Clock Edge	3rd Clock Edge	4th Clock Edge	1st Clock Edge	2nd Clock Edge	3rd Clock Edge	4th Clock Edge
D0	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
D1	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
D2	LOW	LOW	LOW	LOW	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]
D3	LOW	LOW	LOW	LOW	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]
D4	LOW	LOW	LOW	LOW	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]
D5	LOW	LOW	LOW	LOW	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]
D6	LOW	LOW	LOW	LOW	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]
D7	LOW	LOW	LOW	LOW	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]
D8	LOW	LOW	LOW	LOW	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]
D9	LOW	LOW	LOW	LOW	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]
D10	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]
D11	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]
D12	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	LOW	LOW	LOW	LOW
D13	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	LOW	LOW	LOW	LOW
D14	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	LOW	LOW	LOW	LOW
D15	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	LOW	LOW	LOW	LOW
D16	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	LOW	LOW	LOW	LOW
D17	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	LOW	LOW	LOW	LOW
D18	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]	LOW	LOW	LOW	LOW
D19	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]	LOW	LOW	LOW	LOW
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE	DE	DE

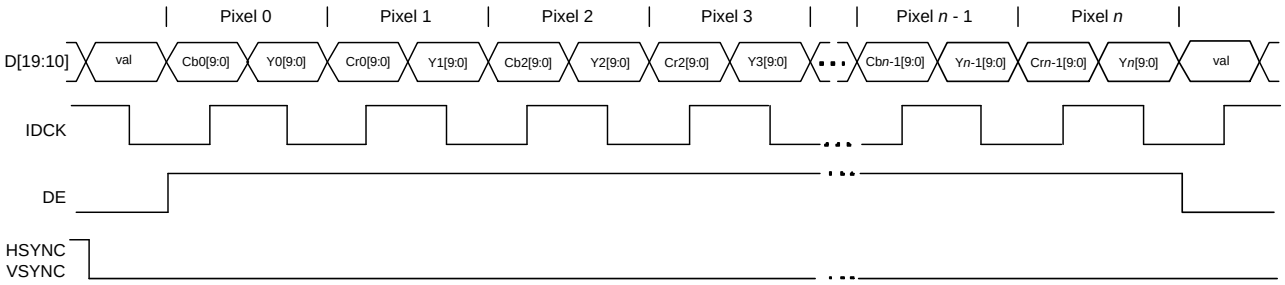


Figure 6.28. 10-bit Color Depth YC Mux 4:2:2 Dual Edge Timing (DRA = 0, YCSWAP = 0)

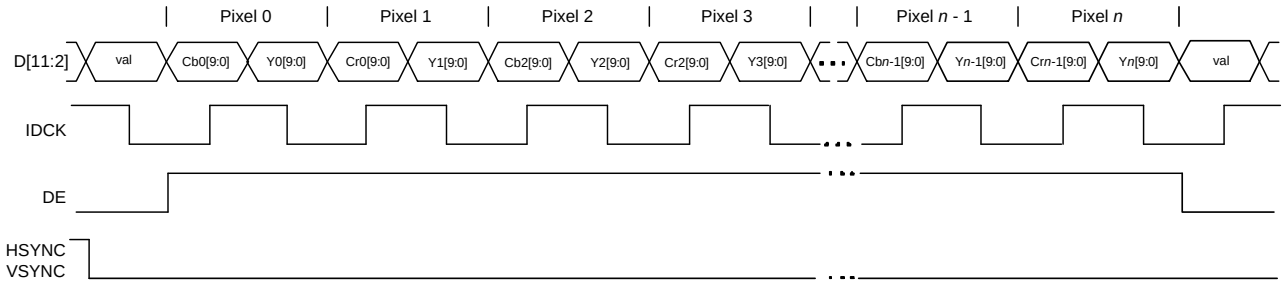


Figure 6.29. 10-bit Color Depth YC Mux 4:2:2 Dual Edge Timing (DRA = 1, YCSWAP = 0)

Table 6.17. YC Mux 4:2:2 12-bit Color Depth Separate Sync Dual Clock Edge Data Mapping

Video Bus Setting	12-bit Data Bus 12-bit Color Depth				12-bit Data Bus 12-bit Color Depth			
YCSWAP	0				0			
DRA	0				1			
Pin Name	Pixel #0		Pixel #1		Pixel #0		Pixel #1	
	1st Clock		2nd Clock		1st Clock		2nd Clock	
	1st Clock Edge	2nd Clock Edge	3rd Clock Edge	4th Clock Edge	1st Clock Edge	2nd Clock Edge	3rd Clock Edge	4th Clock Edge
D0	LOW	LOW	LOW	LOW	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]
D1	LOW	LOW	LOW	LOW	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]
D2	LOW	LOW	LOW	LOW	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]
D3	LOW	LOW	LOW	LOW	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]
D4	LOW	LOW	LOW	LOW	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]
D5	LOW	LOW	LOW	LOW	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]
D6	LOW	LOW	LOW	LOW	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]
D7	LOW	LOW	LOW	LOW	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]
D8	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]
D9	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]
D10	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	Cb0[10]	Y0[10]	Cr0[10]	Y1[10]
D11	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	Cb0[11]	Y0[11]	Cr0[11]	Y1[11]
D12	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	LOW	LOW	LOW	LOW
D13	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	LOW	LOW	LOW	LOW
D14	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	LOW	LOW	LOW	LOW
D15	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	LOW	LOW	LOW	LOW
D16	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]	LOW	LOW	LOW	LOW
D17	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]	LOW	LOW	LOW	LOW
D18	Cb0[10]	Y0[10]	Cr0[10]	Y1[10]	LOW	LOW	LOW	LOW
D19	Cb0[11]	Y0[11]	Cr0[11]	Y1[11]	LOW	LOW	LOW	LOW
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE	DE	DE

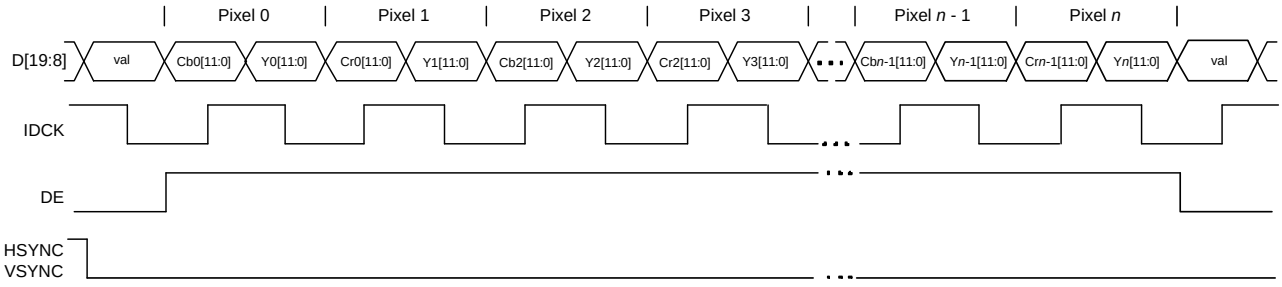


Figure 6.30. 12-bit Color Depth YC Mux 4:2:2 Dual Edge Timing (DRA = 0, YCSWAP = 0)

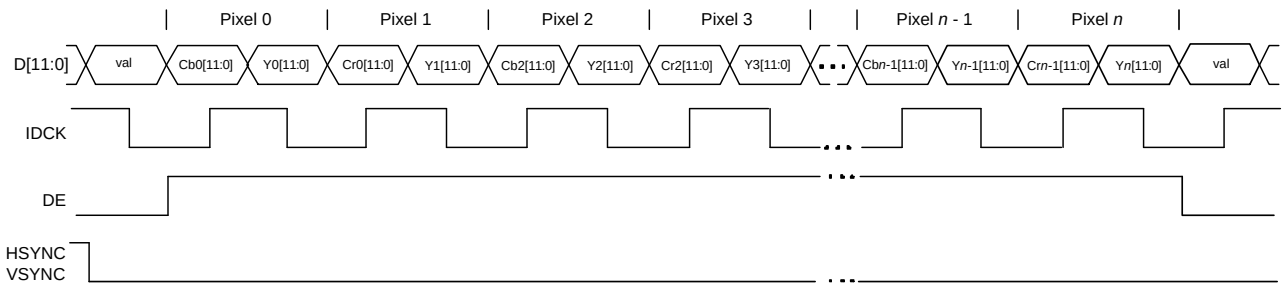


Figure 6.31. 12-bit Color Depth YC Mux 4:2:2 Dual Edge Timing (DRA = 1, YCSWAP = 0)

6.10.8. YC Mux 4:2:2 Embedded Sync Formats Dual Clock Edge

This format is identical to the one described in the YC Mux 4:2:2 Separate Sync Formats Dual Clock Edge section on page 59, except the syncs are embedded and not explicit. The figures following this table show only the first two pixels and last pixel of the line and the SAV and EAV sequences, but the remaining pixels are similar to those shown in the figures of the previous section.

Table 6.18. YC Mux 4:2:2 8-bit Color Depth Embedded Sync Dual Clock Edge Data Mapping

Video Bus Setting	8-bit Data Bus 8-bit Color Depth				8-bit Data Bus 8-bit Color Depth			
YCSWAP	0				1			
DRA	0				1			
Pin Name	Pixel #0		Pixel #1		Pixel #0		Pixel #1	
	1st Clock		2nd Clock		1st Clock		2nd Clock	
	1st Clock Edge	2nd Clock Edge	3rd Clock Edge	4th Clock Edge	1st Clock Edge	2nd Clock Edge	3rd Clock Edge	4th Clock Edge
D0	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
D1	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
D2	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
D3	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
D4	LOW	LOW	LOW	LOW	Y0[0]	Cb0[0]	Y1[0]	Cr0[0]
D5	LOW	LOW	LOW	LOW	Y0[1]	Cb0[1]	Y1[1]	Cr0[1]
D6	LOW	LOW	LOW	LOW	Y0[2]	Cb0[2]	Y1[2]	Cr0[2]
D7	LOW	LOW	LOW	LOW	Y0[3]	Cb0[3]	Y1[3]	Cr0[3]
D8	LOW	LOW	LOW	LOW	Y0[4]	Cb0[4]	Y1[4]	Cr0[4]
D9	LOW	LOW	LOW	LOW	Y0[5]	Cb0[5]	Y1[5]	Cr0[5]
D10	LOW	LOW	LOW	LOW	Y0[6]	Cb0[6]	Y1[6]	Cr0[6]
D11	LOW	LOW	LOW	LOW	Y0[7]	Cb0[7]	Y1[7]	Cr0[7]
D12	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	LOW	LOW	LOW	LOW
D13	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	LOW	LOW	LOW	LOW
D14	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	LOW	LOW	LOW	LOW
D15	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	LOW	LOW	LOW	LOW
D16	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	LOW	LOW	LOW	LOW
D17	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	LOW	LOW	LOW	LOW
D18	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	LOW	LOW	LOW	LOW
D19	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	LOW	LOW	LOW	LOW
HSYNC	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
VSYNC	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
DE	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

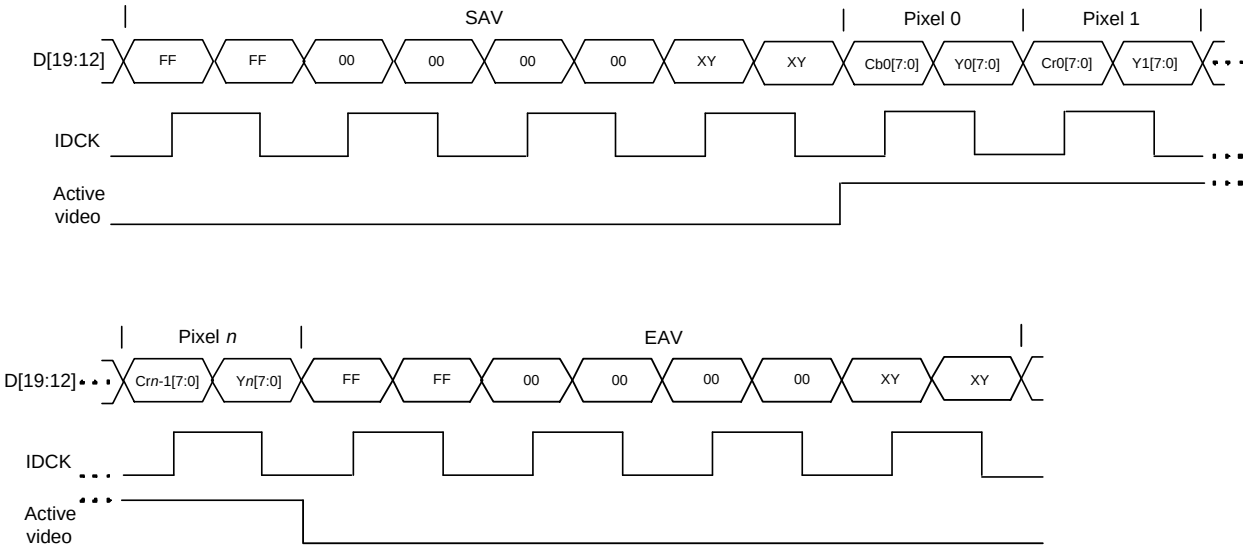


Figure 6.32. 8-bit Color Depth YC Mux 4:2:2 Embedded Sync Dual Edge Timing (DRA = 0, YCSWAP = 0)

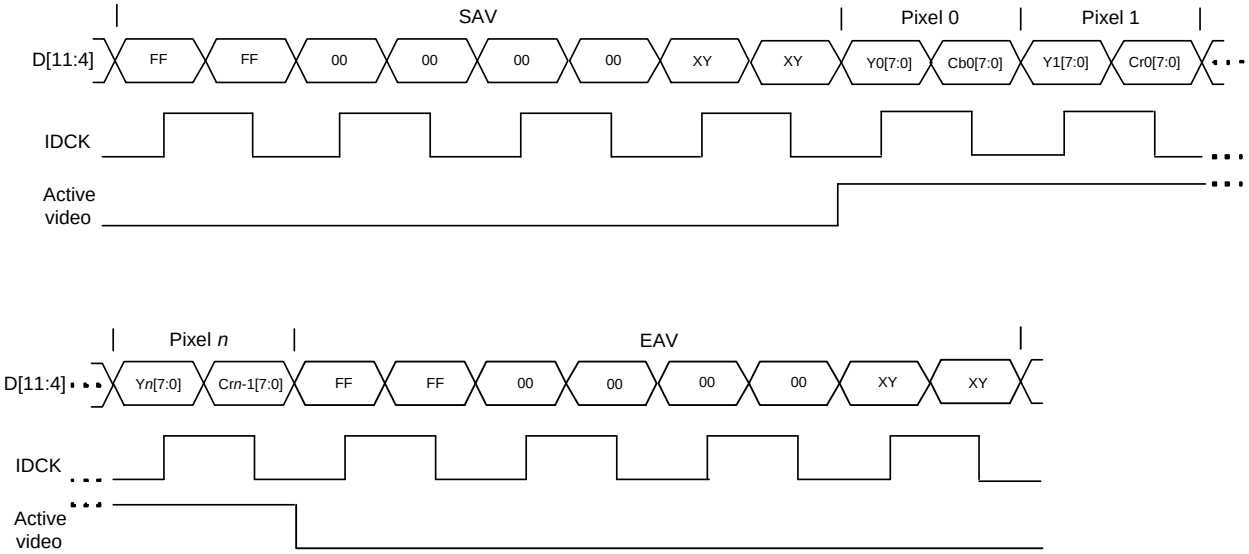


Figure 6.33. 8-bit Color Depth YC Mux 4:2:2 Embedded Sync Dual Edge Timing (DRA = 1, YCSWAP = 1)

Table 6.19. YC Mux 4:2:2 10-bit Color Depth Embedded Sync Dual Clock Edge Data Mapping

Video Bus Setting	10-bit Data Bus 10-bit Color Depth				10-bit Data Bus 10-bit Color Depth			
YCSWAP	0				0			
DRA	0				1			
Pin Name	Pixel #0		Pixel #1		Pixel #0		Pixel #1	
	1st Clock		2nd Clock		1st Clock		2nd Clock	
	1st Clock Edge	2nd Clock Edge	3rd Clock Edge	4th Clock Edge	1st Clock Edge	2nd Clock Edge	3rd Clock Edge	4th Clock Edge
D0	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
D1	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
D2	LOW	LOW	LOW	LOW	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]
D3	LOW	LOW	LOW	LOW	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]
D4	LOW	LOW	LOW	LOW	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]
D5	LOW	LOW	LOW	LOW	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]
D6	LOW	LOW	LOW	LOW	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]
D7	LOW	LOW	LOW	LOW	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]
D8	LOW	LOW	LOW	LOW	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]
D9	LOW	LOW	LOW	LOW	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]
D10	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]
D11	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]
D12	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	LOW	LOW	LOW	LOW
D13	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	LOW	LOW	LOW	LOW
D14	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	LOW	LOW	LOW	LOW
D15	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	LOW	LOW	LOW	LOW
D16	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	LOW	LOW	LOW	LOW
D17	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	LOW	LOW	LOW	LOW
D18	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]	LOW	LOW	LOW	LOW
D19	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]	LOW	LOW	LOW	LOW
HSYNC	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
VSYNC	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
DE	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

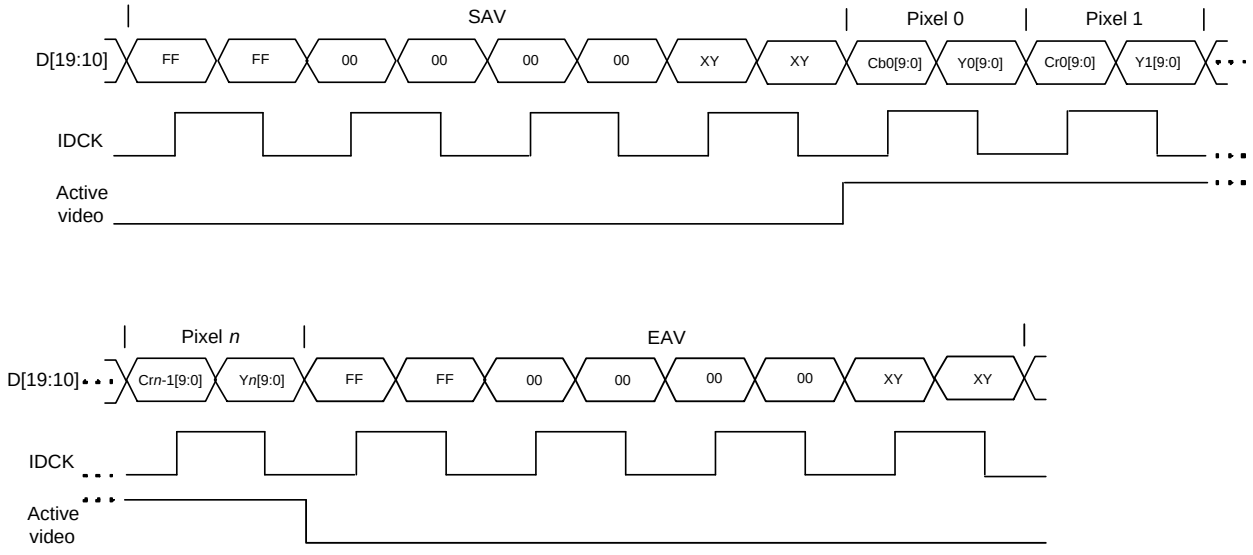


Figure 6.34. 10-bit Color Depth YC Mux 4:2:2 Embedded Sync Dual Edge Timing (DRA = 0, YCSWAP = 0)

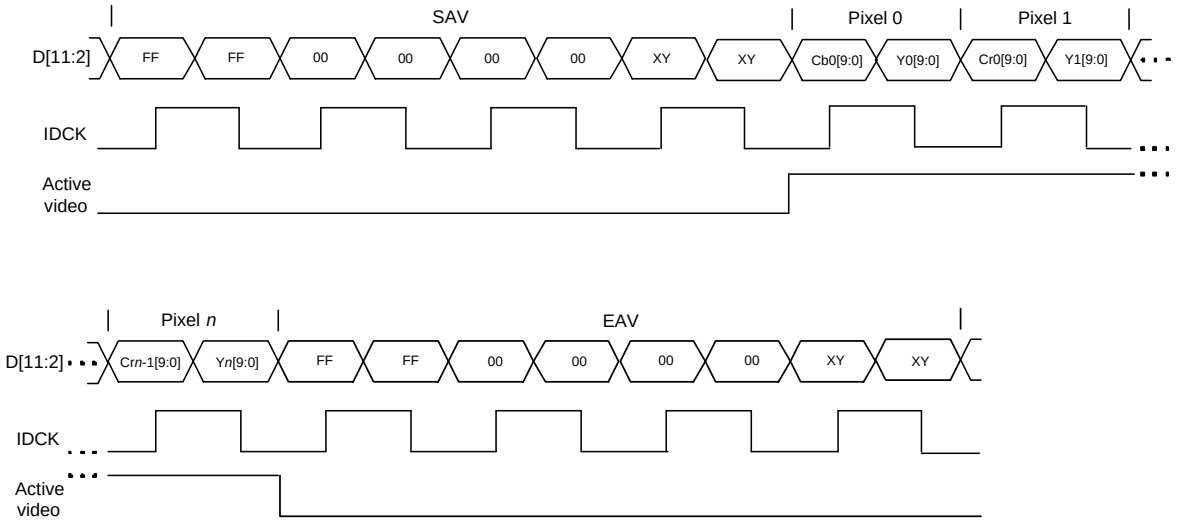


Figure 6.35. 10-bit Color Depth YC Mux 4:2:2 Embedded Sync Dual Edge Timing (DRA = 1, YCSWAP = 0)

Table 6.20. YC Mux 4:2:2 12-bit Color Depth Embedded Sync Dual Clock Edge Data Mapping

Video Bus Setting	12-bit Data Bus 12-bit Color Depth				12-bit Data Bus 12-bit Color Depth			
YCSWAP	0				0			
DRA	0				1			
Pin Name	Pixel #0		Pixel #1		Pixel #0		Pixel #1	
	1st Clock		2nd Clock		1st Clock		2nd Clock	
	1st Clock Edge	2nd Clock Edge	3rd Clock Edge	4th Clock Edge	1st Clock Edge	2nd Clock Edge	3rd Clock Edge	4th Clock Edge
D0	LOW	LOW	LOW	LOW	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]
D1	LOW	LOW	LOW	LOW	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]
D2	LOW	LOW	LOW	LOW	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]
D3	LOW	LOW	LOW	LOW	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]
D4	LOW	LOW	LOW	LOW	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]
D5	LOW	LOW	LOW	LOW	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]
D6	LOW	LOW	LOW	LOW	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]
D7	LOW	LOW	LOW	LOW	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]
D8	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]
D9	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]
D10	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	Cb0[10]	Y0[10]	Cr0[10]	Y1[10]
D11	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	Cb0[11]	Y0[11]	Cr0[11]	Y1[11]
D12	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	LOW	LOW	LOW	LOW
D13	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	LOW	LOW	LOW	LOW
D14	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	LOW	LOW	LOW	LOW
D15	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	LOW	LOW	LOW	LOW
D16	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]	LOW	LOW	LOW	LOW
D17	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]	LOW	LOW	LOW	LOW
D18	Cb0[10]	Y0[10]	Cr0[10]	Y1[10]	LOW	LOW	LOW	LOW
D19	Cb0[11]	Y0[11]	Cr0[11]	Y1[11]	LOW	LOW	LOW	LOW
HSYNC	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
VSYNC	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
DE	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

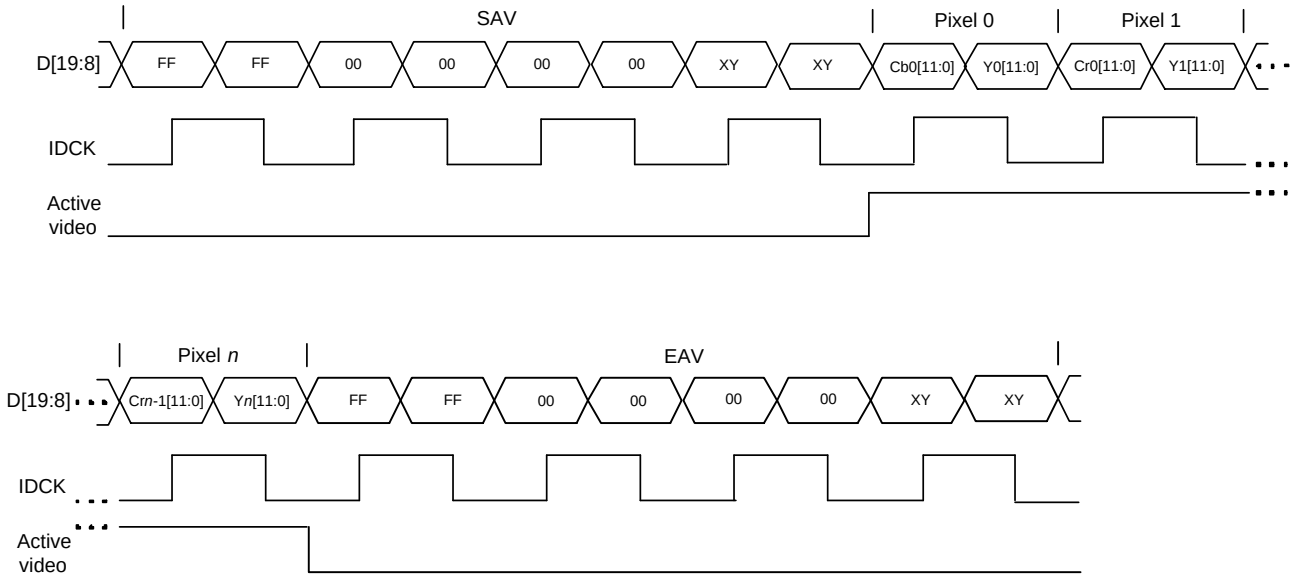


Figure 6.36. 12-bit Color Depth YC Mux 4:2:2 Embedded Sync Dual Edge Timing (DRA = 0, YCSWAP = 0)

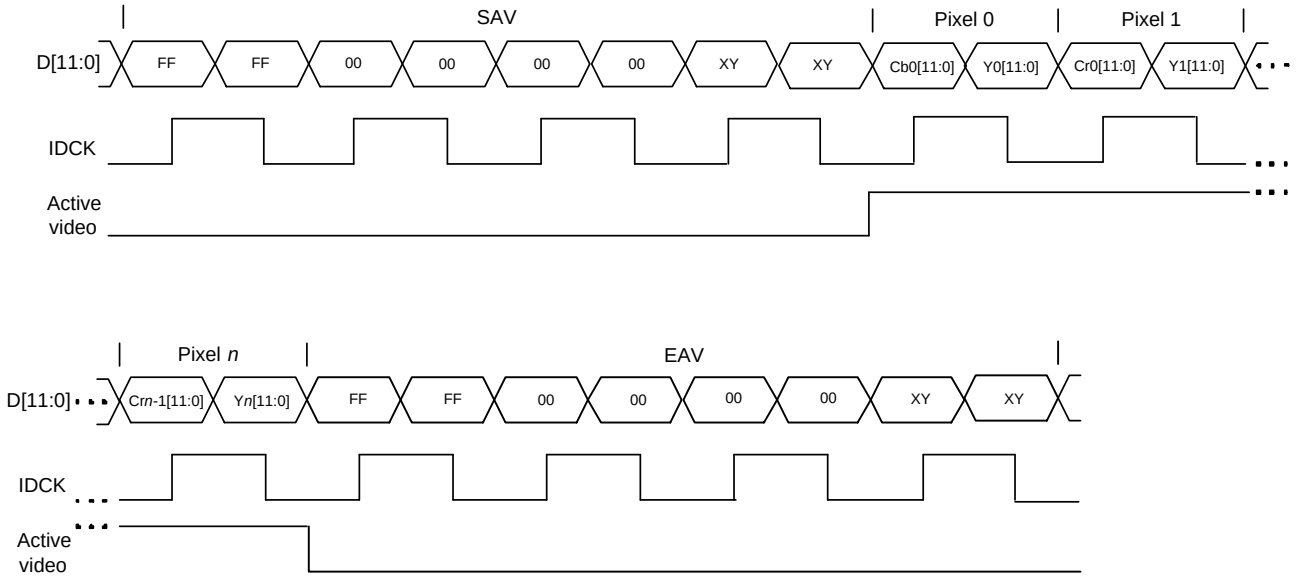


Figure 6.37. 12-bit Color Depth YC Mux 4:2:2 Embedded Sync Dual Edge Timing (DRA = 1, YCSWAP = 0)

7. Design Recommendations

7.1. Power Supply Decoupling

Designers should include decoupling and bypass capacitors at each power signal in the layout. These are shown schematically in Figure 7.1. Connections in one group (such as AVDD33) can share C2, C3, and the ferrite, with each pin having a separate C1 placed as close to the pin as possible. Figure 7.2 is representative of the various types of power connections on the port processor.

The recommended impedance of the ferrite is 10 Ω or more in the frequency range of 1 to 2 MHz.

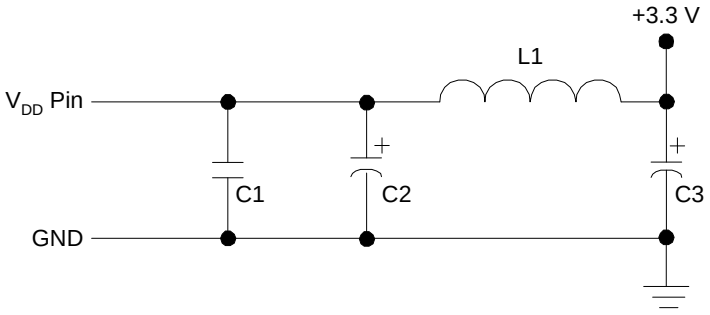


Figure 7.1. Decoupling and Bypass Schematic

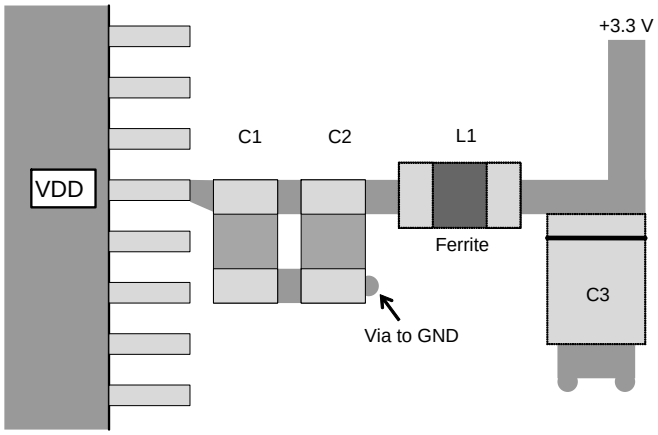


Figure 7.2. Decoupling and Bypass Capacitor Placement

7.2. Power Supply Control Timing and Sequencing

All power supplies in the SiI957n port processor are independent. However, identical supplies must be provided at the same time. For example, all three AVDD33 supplies have to be turned on at the same time.

8. Package Information

8.1. ePad Requirements

The SiI957n device is packaged in a 176-pin, 20 mm × 20mm TQFP package with an exposed pad (ePad) that is used for the electrical ground of the device and for improved thermal transfer characteristics. The ePad dimensions are 7.500 mm × 6.740 mm ±0.20 mm. Soldering the ePad to the ground plane of the PCB is **required** to meet package power dissipation requirements at full speed operation, and to correctly connect the chip circuitry to electrical ground. A clearance of at least 0.25 mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid the possibility of electrical short circuits.

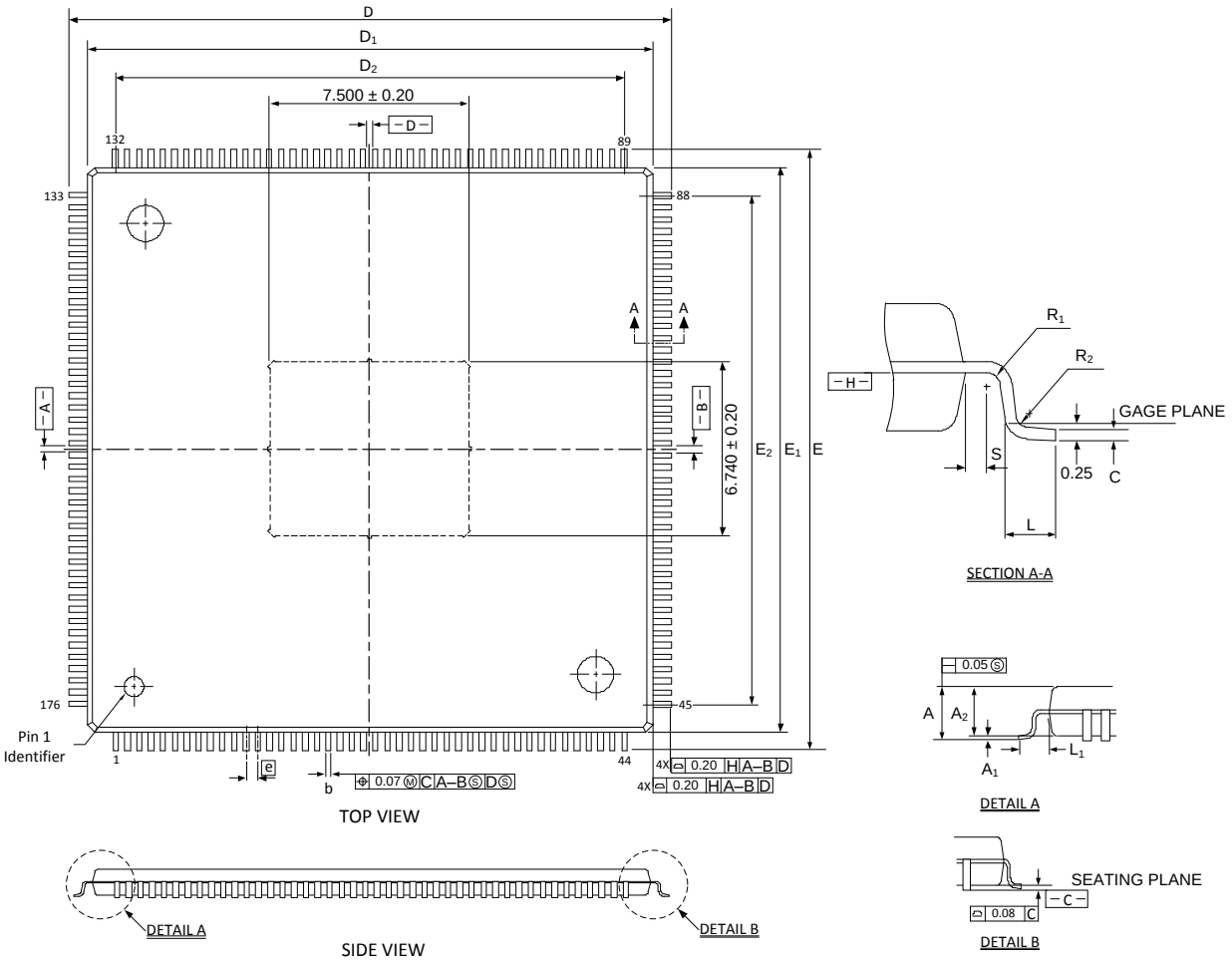
The thermal land area on the PCB may use thermal vias to improve heat removal from the package. These thermal vias also double as the ground connections of the chip and must attach internally in the PCB to the ground plane. An array of vias should be designed into the PCB beneath the package. For optimum thermal performance, the via diameter should be 12 mils to 13 mils (0.30 mm to 0.33 mm) and the via barrel should be plated with 1-ounce copper to plug the via. This design helps to avoid any solder wicking inside the via during the soldering process, which may result in voids in solder between the pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be tented with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 4 mils (0.1 mm) larger than the via diameter.

Package stand-off when mounting the device also needs to be considered. For a nominal stand-off of approximately 0.1 mm, the stencil thickness of 5 mils to 8 mils should provide a good solder joint between the ePad and the thermal land.

Figure 8.1 on the next page shows the package dimensions of the SiI957n port processor.

8.2. Package Dimensions

These drawings are not to scale. All dimensions are in millimeters.



JEDEC Package Code MS-026

Item	Description	Min	Typ	Max
A	Thickness	1.00	1.10	1.20
A1	Stand-off	0.05	0.10	0.15
A2	Body thickness	0.95	1.00	1.05
D	Footprint		22.00 BSC	
E	Footprint		22.00 BSC	
D_1	Body size		20.00 BSC	
E_1	Body size		20.00 BSC	
D_2	—	—	17.20	—
E_2	—	—	17.20	—

Item	Description	Min	Typ	Max
b	Lead width	—	0.16	—
C	Lead thickness	0.09	—	0.20
e	Lead pitch		0.40 BSC	
L	Lead foot length	0.45	0.60	0.75
L_1	Total lead length		1.00 REF	
R_1	Lead radius, inside	0.08	—	—
R_2	Lead radius, outside	0.08	—	0.20
S	Lead horizontal run	0.20	—	—

Figure 8.1. Package Diagram

8.3. Marking Specification

Figure 8.2 shows the markings of the SiI957n package. This drawing is not to scale.

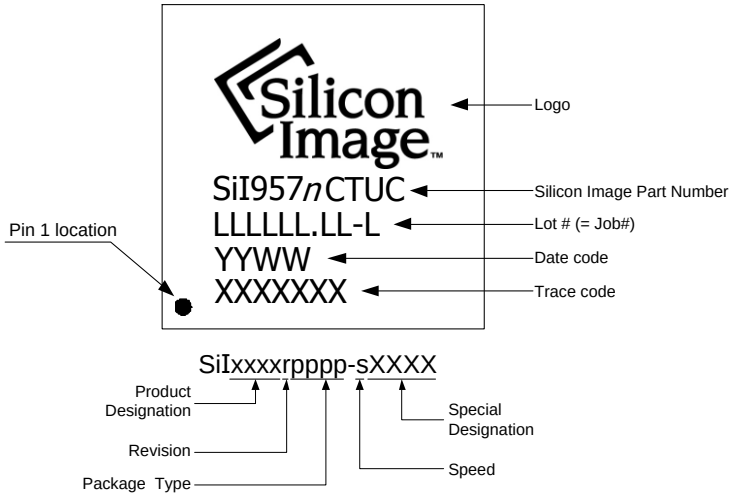


Figure 8.2. Marking Diagram

8.4. Ordering Information

Production Part Numbers:

Device	Part Number
Standard	SiI9573CTUC
With ViaPort Matrix Switch	SiI9575CTUC

References

Standards Documents

This is a list of standards abbreviations appearing in this document, and references to their respective specifications documents.

Abbreviation	Standards publication, organization, and date
HDMI	*High Definition Multimedia Interface*, Revision 1.4a, HDMI Licensing, LLC, March 2010
HCTS	*HDMI Compliance Test Specification,* Revision 1.4a, HDMI Licensing, LLC, March 2010
HDCP	*High-bandwidth Digital Content Protection*, Revision 1.4, Digital Content Protection, LLC; July 2009
DVI	*Digital Visual Interface, Revision 1.0*, Digital Display Working Group; April 1999
E-EDID	*Enhanced Extended Display Identification Data Standard,* Release A Revision 1, VESA; Feb. 2000
E-DID IG	*VESA EDID Implementation Guide*, VESA, June 2001
EDDC	*Enhanced Display Data Channel Standard, Version 1.1,* VESA; March 2004
MHL	*MHL (Mobile High-Definition Link) Specification*, Version 1.2, MHL, LLC, June 2010

Standards Groups

For information on the specifications that apply to this document, contact the responsible standards groups appearing on this list.

Standards Group	Web URL
ANSI/EIA/CEA	http://global.ihs.com
VESA	http://www.vesa.org
HDCP	http://www.digital-cp.com
DVI	http://www.ddwg.org
HDMI	http://www.hdmi.org
MHL	http://www.mhlconsortium.org

Lattice Semiconductor Documents

This is a list of the related documents that are available from your Lattice Semiconductor sales representative.
The Programmer Reference requires an NDA with Lattice Semiconductor.

Document	Title
SiI-PR-1054	*Sil9573, Sil9575, and Sil9523 Port Processor Programmer's Reference*
SiI-PR-0041	*CEC Programming Interface (CPI) Programmer's Reference*

Technical Support

For assistance, submit a technical support case at www.latticesemi.com/techsupport.

Revision History

Revision F, March 2016

Updated to latest template.

Revision F, December 2013

- Added 4K × 2K 50/60 FPS support.
- Added new section on Support for UltraHD resolution at 50P/60P frames per second.

Revision E, September 2013

- Removed statement of “only” on OSD resolution limitations in On-screen Display Controller section.
- Added Note 2 and updated to Note 3 in Table 3.2. Updated current values in Table 3.11: $I_{AVDDI13}$ from 240 to 250, $I_{AVDDI33}$ from 330 to 345, and I_{CVCC13} from 650 to 680 mA.
- Updated Note 3 in Table 3.11 from “three 225 MHz” to “six 300 MHz.”

Revision D, May 2013

Added information about I^2C setup time.

Revision C, January 2013

Updated OSD video support and SBVCC5 voltage measurement; added VS insertion description.

Revision B, August 2012

Updated 3D L/R section, and Table 7; global grammatical changes.

Revision A, January 2012

First production release.

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